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2026 TPCA: tighter supply with innovations underway

Supply of substrate, equipment, glass fiber cloth, and copper foil to all get tighter; new technologies under development

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First impressions from 2026 IMPACT and TPCA – shortages getting worse everywhere

We attended the International Microsystems, Packaging, Assembly and Circuits Technology Conference (**IMPACT**-IAAC) and the Taiwan Printed Circuit Association (**TPCA**) Show in Taipei between 19 and 22 October. The first impression we had during our visit was that the supply of materials and various critical equipment tools has become much tighter than a year ago. For example, for IC substrates, the shortage in low-CTE glass fabric (T-glass) continues to be a concern. Although Nittobo (3110 JP, Not rated) expects to more than double its **"thick" T-glass** capacity in FY28E vs FY26 (*Fig. 1*), the company thinks it is natural that its share in the T-glass market could still trend down through FY30E, echoing Prismark's view (*Fig. 2*) and finds the outcome acceptable since the demand volume is too high to be fulfilled by Nittobo alone while the multi-core trend also accelerates T-glass demand. In our interviews with Nittobo, Taiwan Glass (1802 TT, Not rated), and copper clad laminate (CCL) companies, the most severe bottleneck of glass fiber cloth could lie in the availability of **weaving machinery** from Toyota Industries (unlisted) and **the lead time now extends to five years (until 2031-32), vs last year** when the lead time was until 2029-30. Tsudakoma's (6217 JP, Not rated) looms do not seem to meet the industry standards yet, as per our conversation with glass fiber makers. The constraint of glass fiber cloth expansion not only affects IC substrate, but also PCB/HDI (high-density interconnect). During our interactions in the TPCA, most people agreed that **lower-end electronic-grade glass (E-glass) shortage with monthly price hikes will continue through 1H27E, if not longer**. Furthermore, the shrinking price gap between E-glass and low-Dk1 glass may likely **push up the prices of low-Dk1 glass fiber cloth later this year**, when suppliers switch their capacity back and forth between E- and low-Dk1 glass, given that the total supply is capped by equipment tools.

In addition to **our expectation of tightness in the supply of higher-end copper foil, such as HVLP3 and 4**, along with new AI platforms ramping in 2H26F, we noticed that **lower-end copper foils**, for consumer products and general servers, **are emerging as a new bottleneck for CCL and PCB now**, as copper foil makers are ramping down or ceasing production of legacy products and focusing on higher-end HVLP (hyper very low profile).

We summarize several equipment tools for which lead times have substantially lengthened in the past year in *Fig. 5*, such as **loom equipment** from 3 years (a year ago) to 5 years, **laser drilling** from 1 year to 3 years, **substrate exposure** from 1 year to 3-5 years, and **Ajinomoto build-up film (ABF) vacuum laminator** from <6 months, to 2.5 years.

IC substrates: shortage of higher-end ABF substrates could get worse, with new innovations underway

According to Prismark, the entire ABF substrate market is in a glut, but if we only look at higher-end ABF substrates, the supply shortage is likely to get worse in coming years (*Fig. 3* and *Fig. 4*), given the above-mentioned material and equipment constraint, as well as various upgrade trends. The roadmaps from Kinsus (3189 TT, Not rated), AT&S (ATS AV, Not rated), Shinko (unlisted), and Unimicron (3037 TT, Buy) are shown in *Fig. 7* to *Fig. 12*. **All roadmaps point to the trends of larger body sizes, higher layer counts, embedded active/passive components, multi-core designs, miniaturization of line space/line width (LS/LW) and pitches, etc.** Current high-end substrates in production are around 90x100mm (e.g., stack-up: 10/12+2+10/12 or 8+6+8) with L/S at 8/8um or 9/12um, and we notice NPI projects could be 120x120~150mm (stack-up: 18+2+18 or 10/12+4/6+10/12) with L/S at 5/7um or 5/5um and embedded components in core and ABF layers for 2027F/28F. For advanced testing vehicles, a roadmap of multi-core substrate to 230x150mm (14+n+14) in 2027 and 230x230mm (16+n+16) in 2028E is underway, according to the companies.

In order to achieve those goals, various low-CTE, low-loss material and process innovations (such

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See Appendix A-1 for analyst certification, important disclosures and the status of non-US analysts.

as **glass core, EMIB-T, multi-layer core [MLC], embedded passive/active/power components, various fillers to resin**) are underway.

For example, we have observed **the growing effort on glass core developments this year** (e.g., evident from the presentations of Shinko, AT&S, FICT [unlisted], Toppan [7911 JP, Buy], and TPK [3673 TT, Neutral]) versus last year, as its features of low CTE, low loss, and panel size manufacturing are suitable for future large body size and high performance requirements of future substrates (especially after CoPoS materializes). We believe the two key challenges in glass-core through-glass via (TGV) manufacturing are still **SeWaRe and reliability issues,** while most suppliers are still in R&D stage to solve those issues. Recently, Kinsus highlighted its **aluminum nitride (AlN) ceramic core substrate encountered reliability issues in ABF layers during < -40°C tests**. Compared with glass, AlN is harder to break, with lower distortion (high flexural strength) and higher thermal conductivity, but possesses higher Dk as a trade-off. We believe glass core substrates still have some way to go before commercialization, as even ceramic cores are still facing challenges.

MLC is also a practical solution to enhance the **structural rigidity of** the current organic substrate structure for larger body size and embedded component trends.

Intel (INTC US, Not rated) talked about a **14-bridge EMIB-T package test vehicle** that demonstrated performance scaling in high-speed I/O and power delivery. Intel continues to scale its EMIB-T bump pitch from 45um to 35um with multiple test vehicles, and a 25um program is in the pipeline. It also seeks to scale the package form factor, including test vehicle sizing to a quarter of a 510x515mm working panel containing >200 embedded bridges inside the substrate. Other than Intel, we observed that many suppliers avoided mentioning EMIB-T developments in IMPACT and TPCA. We think it is likely because the technology is specifically tied up with Google's (GOOG US, Not rated) TPU v9 at this moment, and it is sensitive to publicly discuss the details.

PCB/HDI: copper foil shortage may come soon, and debates between PTFE and HCR are here to stay; "embedding" emerges in optical module mSAP HDI

While copper foil supply does not seem to be an issue in 2026, we learnt from CCL vendors that supply could become tighter in coming quarters, **across high tiers**, driven by ramp-up of new AI platforms, **and low tiers**, because of legacy foil capacity conversion of leading copper foil makers looking to support high-end products. We compile major HVLP copper foil makers' capacity planning in *Fig. 37*. We believe some low-grade CCL vendors could look to introduce more Chinese suppliers like Defu (301511 CH, Not rated) and Tongguan (301217 CH, Not rated). Within high-speed CCL, resin selection (**hydrocarbon resin [HCR] or polytetrafluoroethylene [PTFE]**) could dictate CCL makers' upcoming development routes, and we have seen SYTECH (600183 CH, Buy) and TUC (6274 TT, Buy) each introduce PTFE to their roadmap beyond M9/M10 vs. EMC (2383 TT, Buy), Doosan (000150 KS, Not rated) and Nanya (1303 TT, Not rated) remain in the HCR camp. We have a summary of CCL material grade roadmap in *Fig. 35*. The resin debate could drive a growing importance in **filler** selection decision to make up for the physical property shortfall of each material.

A hybrid system (PTFE+HCR) is one of the approaches to balance the advantages of PTFE and HCR, and yet there are several inherent PCB processing problems for pure/hybrid PTFE systems to consider, with and without fiber cloth: 1) hybrid curing/lamination; 2) desmear; 3) drilling; 4) interface bonding; 5) dimension stability and registration; and 6) HDI/sequential lamination designs. Meanwhile, our conversations with some PTFE board makers suggest no particularly significant difference between the electrical performance of HCR and hybrid PTFE, and thermal expansion stability is extremely difficult to control for cloth-less solution. While PTFE board makers think high-temperature lamination equipment is not a must (yet simplifying the production parameter adjustments), they share concerns with lamination and desmear. The development of PTFE manufacturability is worth monitoring, and we believe PTFE vs HCR will be relentless down the road.

For PCB/HDI equipment, we believe the lead time for plating and mechanical drilling is around six months on average, but CO_2 laser drilling delivery could take three years amid demand growth from both HDI and ABF substrate makers. Lamination press lead time also appears to have lengthened to 10 months or more, given rapid backlog growth even without PTFE with only a few vendors and rather small-scale capacity.

Optical module is a growing demand segment for modified semi-additive process (mSAP) HDI, and **near-package optics (NPO) require at least a 16-18L mSAP HDI board**, vs **12-16L mSAP for 1.6T pluggable and 10-12L mSAP for the 800G pluggable optical module**. **Embedded silicon capacitor (Si-cap)** is a trend in optical module boards, which we believe can resolve the insufficient surface issue for increased components in future products and can let high-frequency capacitors

(e.g., Si-cap) process high-frequency signals. ZDT's (4958 TT, Buy) track records in embedding active ICs inside mSAP could be its competitive edge. Considering the transmission distance, **M7/M8/M8.5 materials could be near-term sweet spots** for optical modules, in our view.

AI PCB/CCL project updates: 2H27F trending to M9K1/K2 with more HDI structures

As shown in *Fig. 34* , given the rising GPU/ASIC performance and lower signal loss requirements in the next-gen AI server platforms, we expect new AI GPU/ASIC platforms to increasingly adopt M9K1/K2 CCL (mixed with M4/M6) as mainstream in 2H27-2028F, vs the current generation M8K1/K2 mixed with M4/M6, while the PCB structure will move from high layer count (HLC), M+N, to more HDI (HDI+3-6) or HDI mixed with an M+N structure. It's widely expected that nVidia (NVDA US, Not rated) will stick with HDI+5 for its compute boards for Rubin Ultra. We believe more ASIC or non-nVidia GPUs will adopt NPO for scale-up/out, and this will also accelerate the adoption of high layer count HDI for switches and compute boards. We do not see broadening adoption of Q glass aside from the existing Rubin HGX UBB and LPU in 2027F, likely due to the difficulty of PCB manufacturing processes and the availability of M10 resin. We are still waiting to see if PTFE+HCR or HCR+HCR will be adopted in Rubin Ultra's new switch boards in 2H27F, and it will not be confirmed this early. We see EMC is still the major CCL supplier across all major AI platforms, and Nanya is emerging as a newcomer at a time when end-customers are looking for alternative suppliers, given the tight supply in all the high-end CCL providers. We believe the migration to HDI trend is positive for VGT (300476 CH, Buy), ZDT, Unimicron, and WUS (002463 CH, Buy), while most HLC PCB producers are trying to enhance their HDI capabilities.

Investment summary: Reiterate Buy on Unimicron in ABF substrate; ZDT, Compeq, SCC, VGT, and Shengyi Electronics in PCB/HDI; EMC and SYTECH in CCL

In the ABF substrate space, we reiterate our Buy rating on **Unimicron (3037 TT)**, which is benefiting from more favorable pricing conditions amid supply bottlenecks and technological advancements (EMIB-T with manageable risk-reward, large reticle-size 2.5D, embedding/MLC, etc.). The latter could be crucial in this AI-driven upcycle, as higher substrate technology contents could further extend the lead between tier-1 makers and others for a more favorable competitive landscape, in our view.

For the PCB/HDI sector, we reiterate our Buy ratings on **ZDT (4958 TT)** and **Compeq (2313 TT)**. We think the strong growth of optical module mSAP boards will be margin-accretive growth drivers for ZDT and Compeq. ZDT is also an emerging AI PCB/HDI maker, and is well positioned to penetrate into nVidia, Google, and AWS's (AMZN US, Not rated) PCB/HDI more meaningfully from 2H26F, in our view. Despite the marginal exposure to AI PCB/HDI at this moment, Compeq is a leading HLC+HDI supplier for satellite and ground terminal boards, and we believe Compeq will continue to sustain its leading position in next-gen (V3) space satellite PCBs at substantially higher contents vs. the incumbent (V2). We like **Shennan Circuits (SCC; 002916 CH, Buy)** as one of the key HLC PCB suppliers in the high-end network switch and optical transceiver market; moreover, the company is leveraging its technology knowhow in telecommunication PCB products to work on PTFE PCB applications. We also like **Victory Giant (VGT; 300476 CH/2476 HK, Buy)** for its leading position in the HDI market, which may help the company to benefit from nVidia's strong demand for HDI products, and potential HDI adoption in Google's AI platforms in the future.

Within the CCL sector, we reiterate Buy on **EMC (2383 TT)** and believe EMC is well-positioned to benefit from material upgrades and strong underlying demand in AI PCB given its large capacity scale and ongoing expansion plan over 2027-28F. Additionally, we are comfortable with EMC's leading position in HDI materials which would become strategically more important when AI mainboards begin to move toward HDI in 2H27-1H28F, and we notice the HDI migration does not seem to result in a reduction in layer counts vs current HLC designs. While the debate of HCR vs PTFE is unlikely to settle in the near future, concerns about EMC's contents might be overdone, in our view, given that already there is not much contribution from nVidia's AI platforms. We also like **Shengyi Technology (600183 CH, Buy)** for its rising exposure in the global AI CCL market, and the company is making solid progress in the PTFE CCL market. Moreover, its PCB subsidiary **Shengyi Electronics (688183 CH, Buy)** is well positioned to benefit from AWS' ASIC (Trainium 3) product upgrade.

2026 TPCA: Supply gets tighter, with new technologies underway

We attended the International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT-IAAC) and Taiwan Printed Circuit Association (TPCA) Show in Taipei between 19 and 22 October. Below are our key takeaways:

IC substrates

Continued T-glass capacity expansion, but weaving machinery availability could be a gating factor

Nittobo remains committed to low CTE glass fabric (T-glass) capacity expansion, and expects to more than double its **"thick" T-glass** capacity in FY28E vs FY26 (*Fig. 1*) by adding more **furnaces for yarns** in Japan and Taiwan. Part of the subsequent weaving is outsourced to Nanya which has a large loom installed base. Despite that, Nittobo thinks its share in the T-glass market could still trend down through FY30E and finds the outcome acceptable since the demand volume is too high to be fulfilled by Nittobo alone (*Fig. 2*). The company's strategy is to focus on key accounts.

For **"thin" T-glass** capacity, Nittobo does not plan to add as much and notes the simplicity of thin fabric production and the capacity fungibility from thick fabric production. Admittedly, multi-layer core (MLC) in Ajinomoto build-up film (ABF) substrates could bring incremental demand for thin T-glass, but Nittobo believes the volume is disproportionate to the consumption growth of thick T-glass in the core layers.

Taiwan Glass is also adding T-glass capacity in Taiwan, but unlike Nittobo, Taiwan Glass does not plan to outsource weaving due to extra qualification efforts that could take two more years. While the company's production yield is improving, the most severe bottleneck could lie in the availability of **weaving machinery** from Toyota Industries and the lead time is extended to five years by our observation. Tsudakoma's looms do not seem to meet the industry standards, as per our conversation with glass fiber makers.

Fig. 1: Nittobo's glass fabric expansion plans



Source: Nittobo, Nomura research

Fig. 2: Nittobo's T-glass share in substrate core could dip



Source: Prismark, Nomura research

Lengthening lead time for critical tools

As the IC substrate body size expands beyond 100x100mm toward >120x120mm with more layer counts (toward >24 layers), substrates are consuming more area per unit, outpacing unit volume growth. Prismark identified that only "high-end substrates" are in supply shortage, whereas "the entire substrate industry" is in a glut (*Fig. 3* and *Fig. 4*).

We observe lead time of several critical tools in advanced IC substrate/material production is generally much longer than 10-12 months ago because of high demand from customer capacity adds and more importantly, relatively slower capacity adds by equipment makers (*Fig. 5*). A speaker from Kinsus flagged that the industry advanced substrate capacity is gated by the slowest qualified input, not by cleanroom floor space, and he believes capex has to be committed **18-24 months** ahead of firm demand visibility given the risk of "qualifying too late" rather than "building too much" (*Fig. 6*).

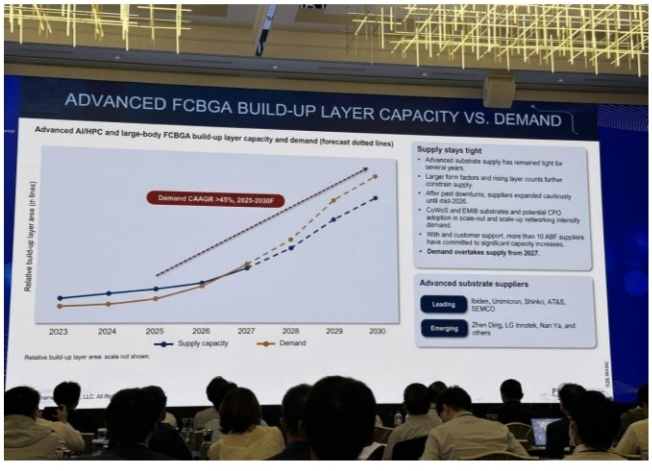
Apart from **Toyota's looms** for T-glass fabrication, **Mitsubishi Electric's** (6503 JP, Buy) **CO_2 laser drilling machine** lead time is currently three years, and the delivery of new **exposure equipment by ORC Manufacturing** (unlisted) is three-to-five years. Compared with our observation during SEMICON Taiwan 2026 (*report*), the lead time of **Nikko Material's** (a subsidiary of Eternal Precision Mechanics [7795 TT, Not rated]) **ABF vacuum laminator** has further risen to 2.5 years, and the monthly production capacity may only reach 28 units by 4Q27E from c.18 units currently.

Fig. 3: Entire ABF substrate industry is in a glut



Source: Prismark, Nomura research

Fig. 4: Only high-end ABF substrate supply is in shortage



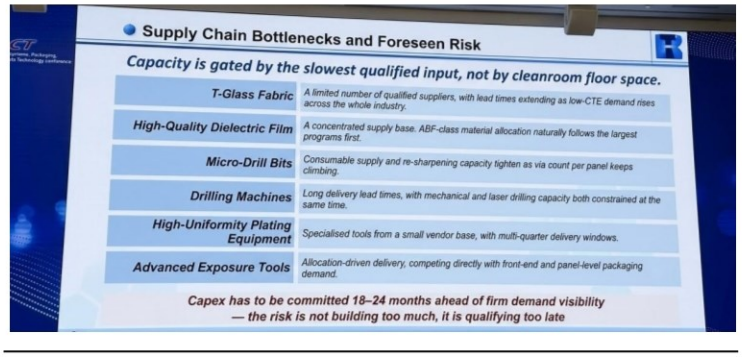
Source: Prismark, Nomura research

Fig. 5: IC substrate critical tool lead time

Equipment	Supplier(s)	Lead time	
		Current	Late 2025/Early 2026
Loom (for T-glass)	Toyota, Tsudakoma?	5 years	~3 years
Laser drilling	Mitsubishi Electric	3 years	12-14 months
Exposure	ORC, SCREEN	3-5 years	12-14 months
ABF vacuum laminator	Nikko Material, JSW?	2.5 years	4-5 months

Source: Company data, Nomura research

Fig. 6: Supply chain bottlenecks of IC substrates

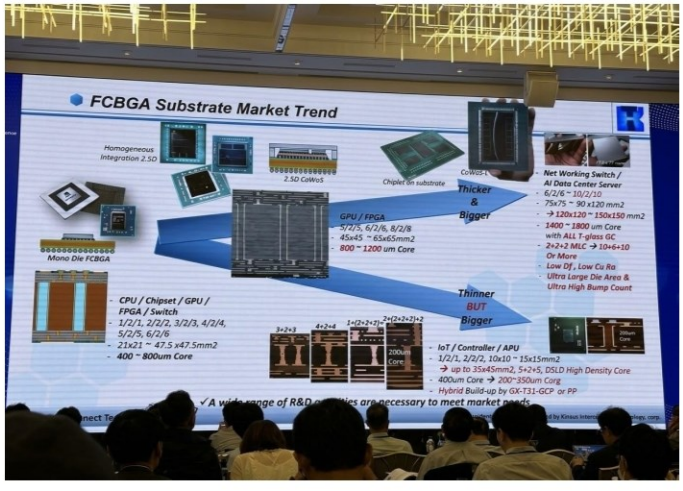


Source: Kinsus, Nomura research

IC substrates are hubs of system integration with embedded technologies

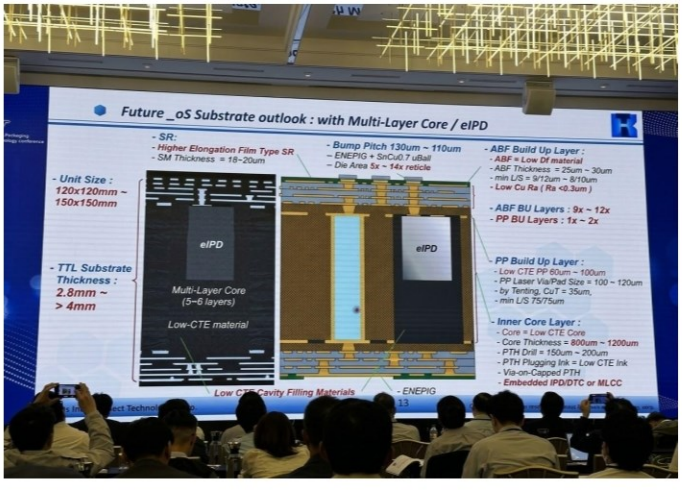
We saw more discussions about large body size substrates in this year's IMPACT seminars, and associated innovations like embedding, MLC, and glass-core were the focus of several conversations as substrates function not just as passive carriers but also active system integration hubs, being part of the power delivery network (PDN) and the thermal path. Embedding components in the build-up or core layers of an IC substrate could enhance the overall signal and power integrity, in our view. Kinsus expects greater adoption of **embedded integrated passive device (IPD)/deep-trenched capacitor (DTC) or MLCC** in the core layer and will build a core layer factory to support embedding and MLC. AT&S also laid out a roadmap to embed components using ABF in larger substrates into 2027-28E. Unimicron currently has passive-embedded (in the core layer) substrate in production with sizes up to 93x93mm (stack-up: 10+2+10 and 8+6+8) and NPI of 120x120mm (stack-up: 18+2+18 and 10+n+10) and unfolded a roadmap to 120x150mm (14+n+14) in 2027E and 150x150mm (16+n+16) in 2028E.

Fig. 7: ABF substrate market trend



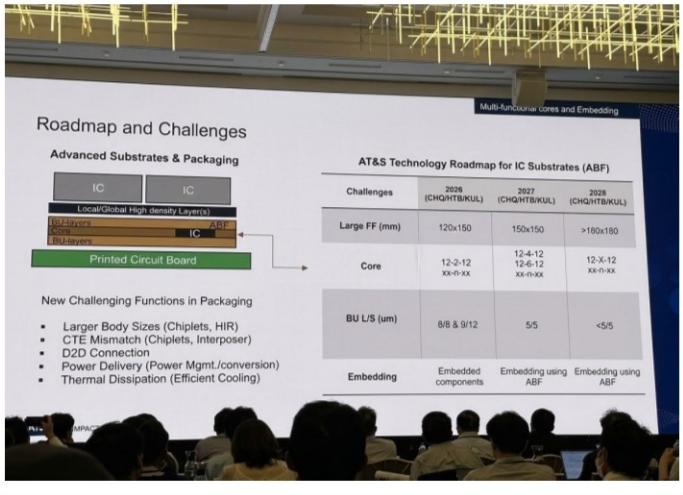
Source: Kinsus, Nomura research

Fig. 8: Embedding and MLC are trends of ABF substrate



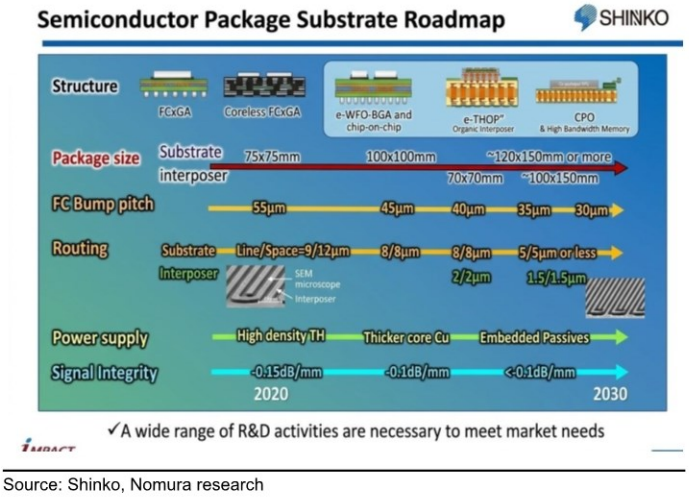
Source: Kinsus, Nomura research

Fig. 9: AT&S substrate technology roadmap



Source: AT&S, Nomura research

Fig. 10: Shinko's substrate technology roadmap



Source: Shinko, Nomura research

Fig. 11: Unimicron's organic substrate roadmap

Feature (unit: um)		2026 HVM	2026 NPI	2027	2028	2029-30
Structure	Stack-up	11-2-11	12-n-12	14-n-14	16-n-16	18-n-18
	Core thickness	400-2,400	2,400	3,000	3,600	3,600
Max body size (mm)		110x110	120x150	150x150	150x230	230x230
Mech drill/pad	0.6-1.2um core	150/250	150/240	120/220	110/200	100/180
Blind via/pad	# of stacked via	5	7	8	9	9
	Laser via (dielectric thickness)	55/80 (25um D)	40/65 (20um D)	35/60 (20um D)	30/55 (15um D)	25/50 (10um D)
Core layer L/S	Subtractive (20um typical Cu)	50/50	40/40	40/40	40/40	40/40
Build-up L/S	SAP ABF	9/12	8/8	5/7	5/5	3/3

Source: Unimicron, Nomura research

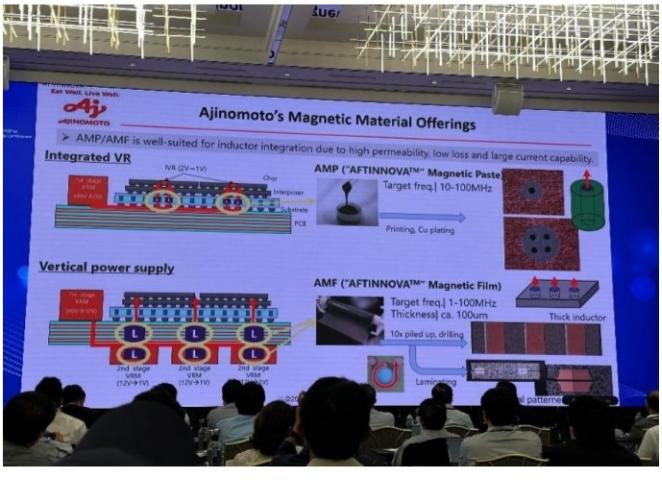
Fig. 12: Unimicron's embedded passive substrate roadmap

Feature (unit: um)		2026 Production	2026 NPI	2027	2028
Structure	Stack-up	10-2-10 8-6-8	10-2-10 10-n-10	14-n-14	16-n-16
Max body size (mm)		93x93	120x120	120x150	150x150
Bump area	Bump pitch	110	90	85	80
	SRO	50	45	45	40
Build-up layer	Line/Space	8/10	7/8		5/5
	Min. via/land diameter	50/75	40/67	40/62	30/55
Core layer	Line/Space	25/25		20/25	
High speed dielectric material loss tangent		0.0034 (10GHz)	0.0022 (10GHz)	0.0020 (10GHz)	
Low roughness Cu treatment		CZ8401		Next gen	

Source: Unimicron, Nomura research

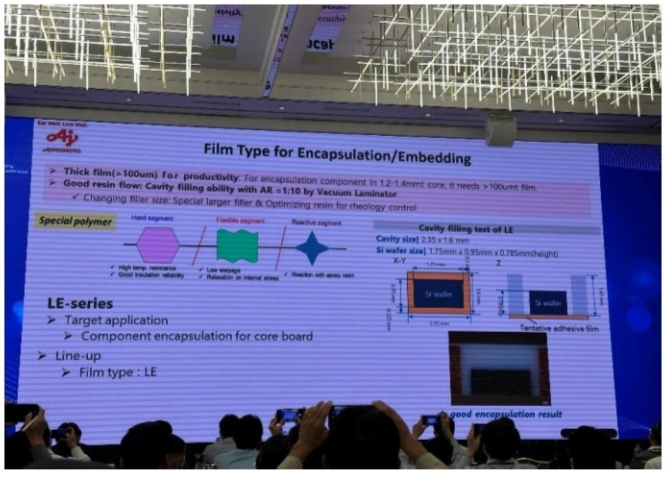
Substrate material vendors also showcased innovative materials in response to the trend of embedding passive components. **Ajinomoto** tailors materials to fabricate discrete inductors for embedding, and paste for integrated inductors within the build-up layers. According to Ajinomoto, its **AFTINNOVA Magnetic Paste (AMP)** and **AFTINNOVA Magnetic Film (AMF)** are well-suited for inductor integration due to high permeability, low loss, and large current capability. Integrated voltage regulators can be established by screen printing to dispense the solvent-free AMP uniformly into substrate cavities and copper electroplating to build the conductive metallic traces over and around the AMP magnetic core. For thick conductors in the voltage regulator module (VRM) in vertical power supply, up to 10 layers of AMF are piled up for subsequent vacuum lamination and heat press, followed by laser drilling and patterning to form VRMs. Additionally, Ajinomoto demonstrated special film-type polymer **LE-series** (thickness >100um), for encapsulation of components in the substrate core (thickness of 1.2-1.4mm), with good resin flow feature to fill cavities.

Fig. 13: Ajinomoto's magnetic materials for embedded PDN



Source: Ajinomoto, Nomura research

Fig. 14: Ajinomoto's encapsulation film for embedding



Source: Ajinomoto, Nomura research

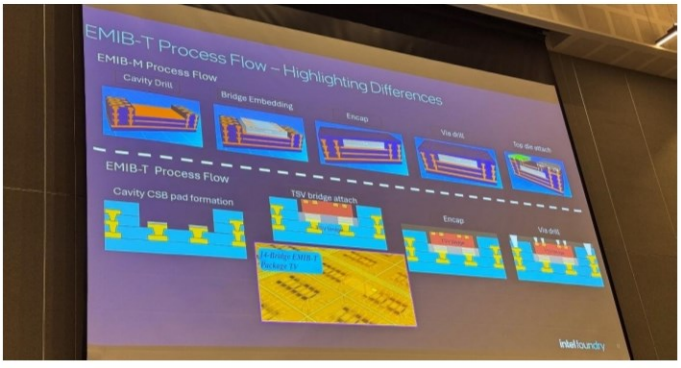
Yet, compared to IMPACT 2025 when a few occasions elaborated on the underlying substrate technologies and advantages of Intel's EMIB-T, we observed much fewer mentions of this patented process in the seminar this year by substrate makers, and believe primary EMIB-T substrate partners could be less vocal given continued development progress for secured projects in the pipeline, especially Google's TPU v9, which we believe will be the litmus test for the technology's execution and economic viability.

Intel talked about a **14-bridge EMIB-T package test vehicle** that demonstrated performance scaling in high-speed I/O (routing density/signal bandwidth) and power delivery (direct current [DC] voltage drop and alternating current [AC] impedance reduction). Intel continues to scale EMIB-T bump pitch from 45um to 35um with multiple test vehicles, and 25um program is in the pipeline. It also seeks to scale the package form factor, including a test vehicle sizing to a quarter of a 510x515mm working panel containing >200 embedded bridges inside the substrate.

Intel's vision is to enable the EMIB-T package substrate to become a versatile platform of

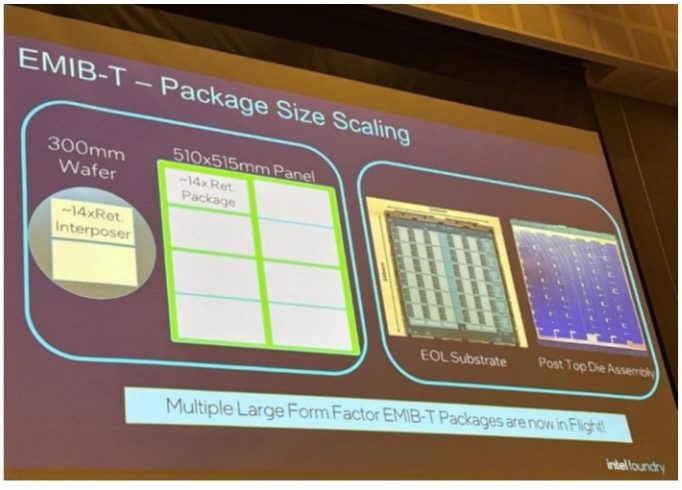
heterogeneous integration, such as: 1) embedding DTC in substrates for further decoupling in high-power devices; 2) utilizing CoaxMIL technology by housing integrated voltage regulators (IVRs) in top silicon and magnetic inductors in substrates; 3) enabling silicon bridges for not only die-to-die communication but also as capacitors; and 3) integration of co-packaged optics (CPO). All told, we believe the deviation of specs from the current AI/HPC substrate structure could lead to **production yield and warpage challenges** given many active/passive components embedded, and it is imperative for Intel and its substrate partners to prove all the technological benefits could be realized in more than just test vehicles.

Fig. 15: EMIB-T vs EMIB-M process flows



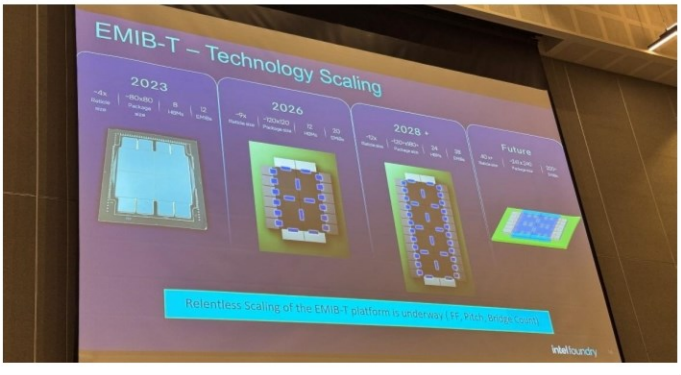
Source: Intel, Nomura research

Fig. 16: EMIB-T package scaling



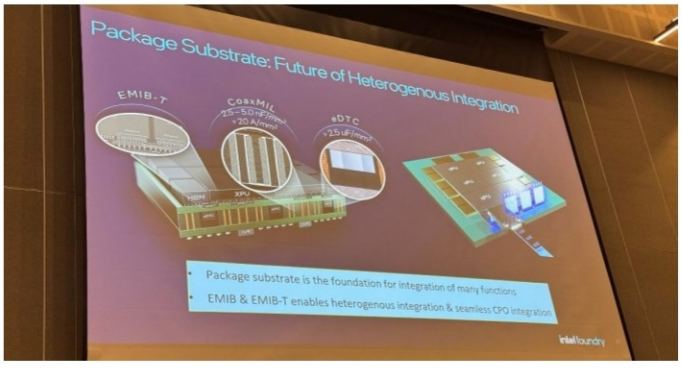
Source: Intel, Nomura research

Fig. 17: EMIB-T technology scaling



Source: Intel, Nomura research

Fig. 18: EMIB-T can be a hub of heterogenous integration



Source: Intel, Nomura research

MLC – from rigidity to possibly functionality

For larger substrates, **Unimicron** current has a max body size of 110x110mm in production with stack-up of 11+2+11/11+6+11 and has incoming designs featuring 120x150mm dimension with stack-up of 12+n+12. The company has laid out a roadmap to 230x150mm (14+n+14) in 2027E and 230x230mm (16+n+16) in 2028E. CPO substrate is also an example of large body size substrate to integrate optical engines (OEs) on top. Unimicron has 110x110mm (9+2+9) in production and NPI of 150x150mm (10+n+10) currently and will introduce 150x150mm (11+n+11) in 2027E and 150x180mm (11+n+11) in 2028E.

Larger substrates could require thicker core layers for **structural rigidity**, and MLC offers an option to thicken copper plane for better power delivery. Extra routing layers of MLC could also provide layout flexibility. Unimicron now has MLC substrates of 9+6+9 in production (110x110mm) and 10+8+10 in NPI (120x150mm) and expects to expand the scope to 14+n+14 for 230x150mm substrates in 2027E and 16+n+16 for 230x230mm substrates in 2028E.

AT&S presented about potential solutions in the core development by moving from pure structural core (2-layer) currently to **functional core for flexibility and design partitioning**, and multi-functional cores in the future. AT&S believes more laser vias per microvia through hole and

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differential drilling could foster better ampacity, and also notes that thicker copper in inner layers could improve power lateral distribution, which is not possible in the build-up layer.

Fig. 19: Unimicron's large body size substrate roadmap

Feature (unit: um)		2026 Production	2026 NPI	2027	2028
Structure		11-2-11 11-6-11	12-n-12	14-n-14	16-n-16
Max body size (mm)		110x110	120x150	230x150	230x230
Bump area	Bump pitch	90	80	70	60
	SRO	45	40	35	30
Build-up layer	Line/Space	9/12	8/8	5/7	5/5
	Min. via/land diameter	55/80	40/65	35/60	30/55
Core layer	Line/Space (mSAP)	25/25	20/25	20/25	20/25
High speed dielectric material loss tangent		0.0034 (10GHz)	0.0022 (10GHz)	0.0020 (10GHz)	
Low roughness Cu treatment		CZ8401	Non-etching	Next gen	

Source: Unimicron, Nomura research

Fig. 20: Unimicron's CPO substrate roadmap

Feature (unit: um)		2026 Production	2026 NPI	2027	2028
Structure		9-2-9	10-n-10	11-n-11	
Max body size (mm)		110x110	150x150		150x180
Bump area	Bump pitch	150	90		80
	SRO	75	45		40
Build-up layer	Line/Space	12/12	9/12		8/8
	Min. via/land diameter	60/90	60/90	60/90	55/85
Core layer	Line/Space	65/65	65/65		
High speed dielectric material loss tangent		0.0036 (5.8GHz)	0.0022 (5.8GHz)	0.0020 (5.8GHz)	
Low roughness Cu treatment		CZ8401	CZ8401 next gen		

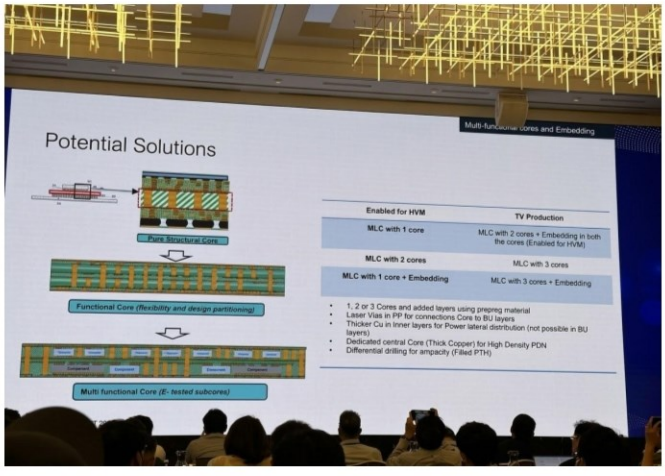
Source: Unimicron, Nomura research

Fig. 21: Unimicron's MLC substrate roadmap

Feature (unit: um)		2026 Production	2026 NPI	2027	2028
Structure		9-6-9	10-8-10	14-n-14	16-n-16
Max body size (mm)		110x110	120x150	230x150	230x230
Board thickness for core layer (mm)		2.4	3.0	3.2	3.6
Overall board thickness (mm)		3.2	4.5	4.7	5.1
Bump area	Bump pitch	150	130		110
	SRO	70	60		55
Build-up layer	Line/Space	14/14	12/12		9/12
	Min. via/land diameter	60/85	50/75	45/70	40/65
Core layer	Line/Space (35um Cu)	75/75	70/70	65/65	60/60
High speed dielectric material loss tangent (@10GHz)		0.0034	0.0034	0.0022	

Source: Unimicron, Nomura research

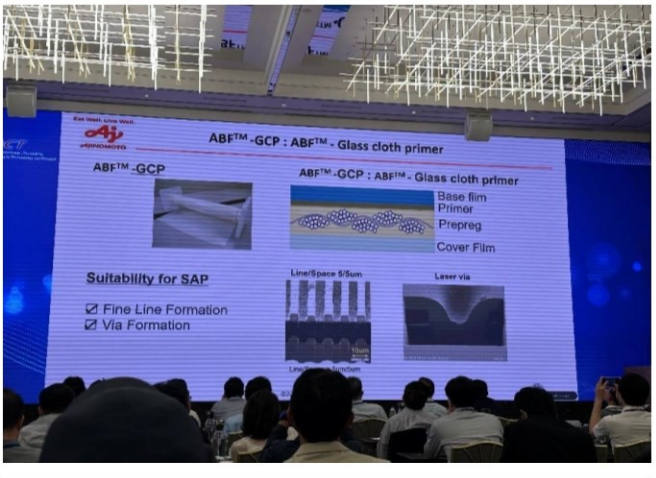
Fig. 22: AT&S proposes (multi-)functional core solutions



Source: AT&S, Nomura research

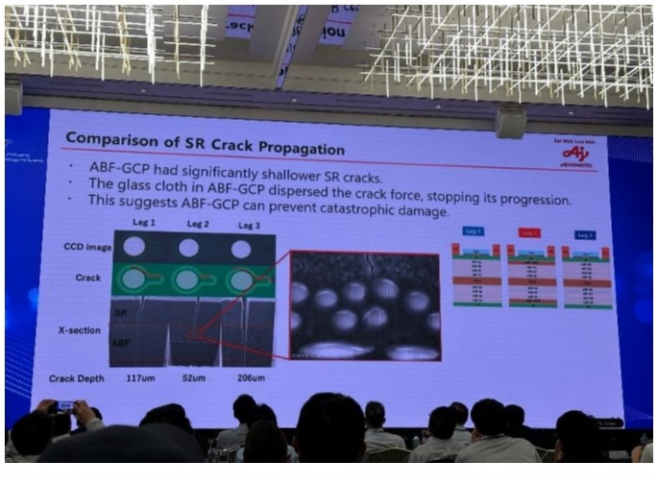
Ajinomoto also presented its **ABF-GCP (glass cloth primer)** that incorporates glass cloth and a primer interface into ABF for mechanical reinforcement when package footprint scales up. ABF-GCP on the top layer can curb solder resist (SR) cracks in Ajinomoto's test, since the glass cloth in ABF-GCP disperses the crack force and stops the propagation. Ajinomoto believes a lower warpage using ABF-GCP can make the strengthened film a solution **before** the real advent of glass-core substrates in large package sizes.

Fig. 23: ABF-GCP



Source: Ajinomoto, Nomura research

Fig. 24: ABF-GCP disperses SR crack force



Source: Ajinomoto, Nomura research

The revival of glass-core substrate discussion?

After a rather muted TPCA Show and IMPACT for through-glass via (TGV) and glass core substrate in 2025, we sensed the topics gained traction in this year's event again. Our discussions with glass solution providers at the TPCA Show suggested that **glass core substrate remains the mainstream application target for TGV.** We highlight some new findings below.

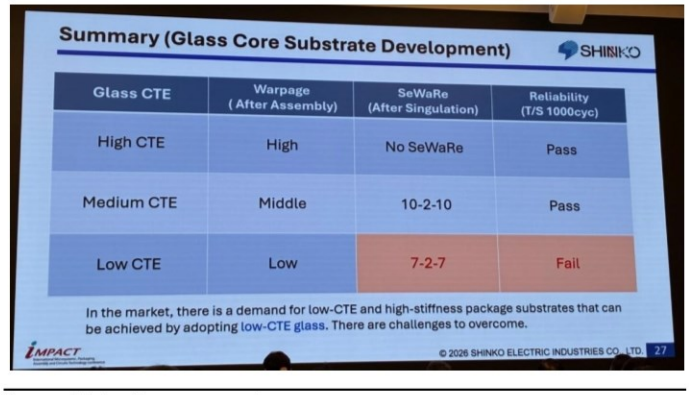
For the first time, **TPK** attended the exhibition and showcased its determination to transform into a TGV foundry and capabilities to handle mechanical laser process and etching by leveraging its established know-how in cover glass and lamination. TPK has opted for a working panel of 300x300mm based on wet process for electroplating and etching and has begun collaboration with OSAT trial lines for qualification, with an aim to kick-off engagement with substrate makers from 2027E.

The two key challenges in TGV manufacturing are **SeWaRe and reliability issue**. SeWaRe is the phenomenon of microcracks or splitting between build up layers and glass core caused by tensile stress from CTE mismatch between build-up resin and glass. These tiny defects can act as stress concentration points during subsequent manufacturing process and lead to larger crack and limit yields. To address SeWaRe, as shown in *Fig. 26*, **Shinko** uses edge coating to contract the tensile stress. Another issue caused by CTE mismatch is the reliability issue. Shinko highlighted larger cracks propagating across TGVs and the glass core for low-CTE glass after 1,000 thermal cycles despite edge coating. To address this, Shinko put an additional buffer layer between build-up resins and glass core, and a relaxation layer inside the via to absorb the tension, but both measure increase process complexity.

Some glass core makers showed their progress on **multilayer glass core substrate**. As shown in *Fig. 28*, the structure comprising two or more TGV glass layers attached by an organic (ABF) layer. This design offers two main advantages: 1) thinner individual glass layers facilitate via formation and metallization while insertion loss remains comparable to that of a single-core structure; 2) the compliant organic layer absorbs strain energy through shear deformation, helping reduce stress concentrations. However, we believe multilayer glass core is still far away, as the additional alignment and lamination processes would add further complexity to TGV technology that is still developing.

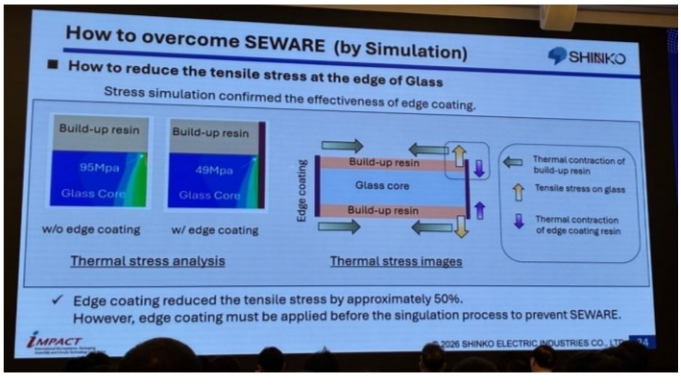
Beyond glass, **Kinsus** also showed its **aluminum nitride (AlN) ceramic core substrate solutions with through-ceramic vias (TCV)**. As shown in *Fig. 29*, compared with glass, AlN is harder to break (higher elastic coefficient and fracture toughness), lower distortion (high flexural strength) and higher thermal conductivity, but possess higher Dk as a trade-off. We believe glass core substrate should still have some way to go before its commercialization, as even ceramic cores are still facing challenges.

Fig. 25: Glass-core substrate development



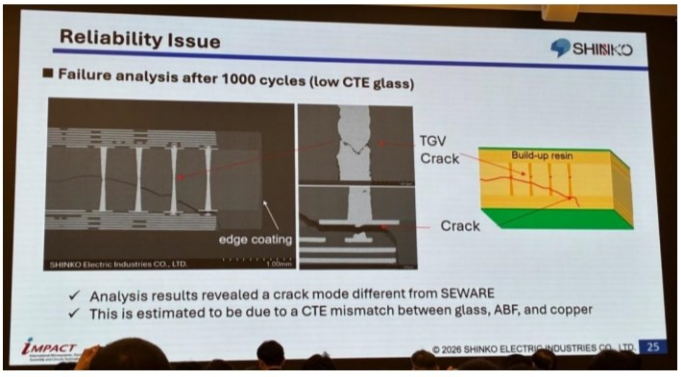
Source: Shinko, Nomura research

Fig. 26: Shinko uses edge coating to counter SeWaRe



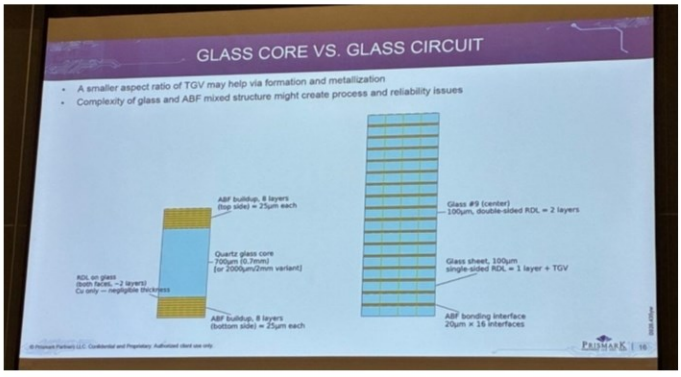
Source: Shinko, Nomura research

Fig. 27: TGV crack leads to reliability issues



Source: Shinko, Nomura research

Fig. 28: Multi-layer glass-core



Source: Prismark, Nomura research

Fig. 29: Core material selection

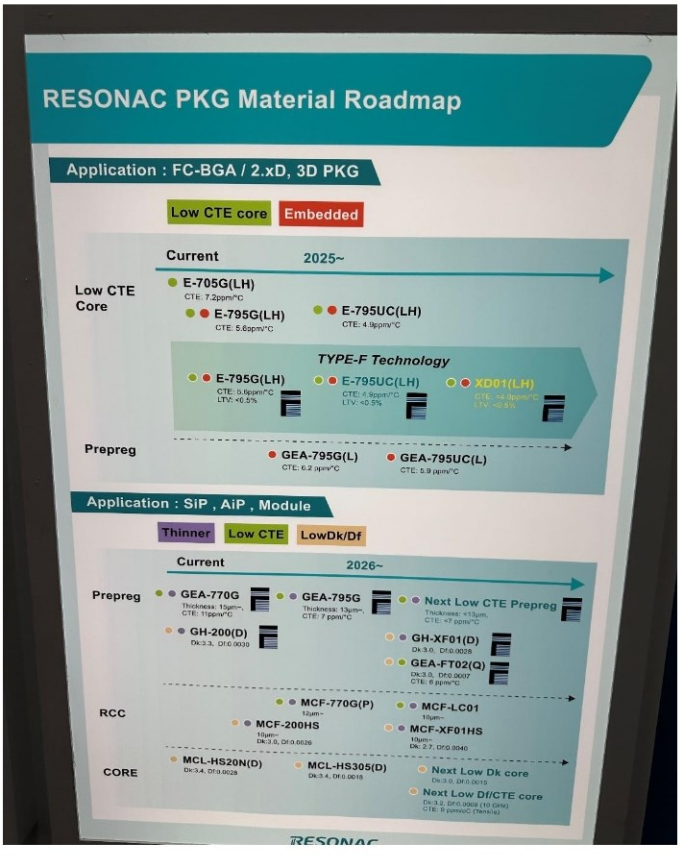
Properties	E795G(LH)	AIN	Glass	Si
Fracture toughness (Mpa*m^0.5)	-	2.6~3.5	0.7~0.9	0.9~1.2
Elastic coefficient (GPa)	32	300~320	60~75	130~185
CTE (ppm/°C)	5.8	4~4.5	3.2~8.5	2.6~3.2
Flextural strength (Mpa)	41	300~400	50~100	120~200
Thermal conductivity (W/m·K)	0.68	170~230	1~1.4	130~150
Specific heat (J/kg·°C)	-	730	800	710
Density (g/cm^3)	-	3.2	2.6	2.32
Melting point (°C)	480	2,200	1,200~1,600	1414
Dk (10GHz)	4.2	8.5~9	4~6	11.7
Df (10GHz)	0.007	<0.001	0.001~0.005	0.005~0.01

Source: Kinsus, Nomura research

Alternative materials for IC substrates

We saw more displays of substrate copper clad laminate (CCL) in this year's exhibition, likely due to supply constraints from the leading player **Resonac** (4004 JP, Buy). The progress of **EMC**'s ABF substrate CCL in an AI ASIC project is worth monitoring, and the qualification outcome is likely to be available in 4Q26F, in our view. Furthermore, there seem to be more queries by Chinese chip designers for domestic build-up films considering that Ajinomoto prioritizes its supply to support overseas end chip clients.

Fig. 30: Resonac's substrate CCL roadmap



Source: Resonac, Nomura research

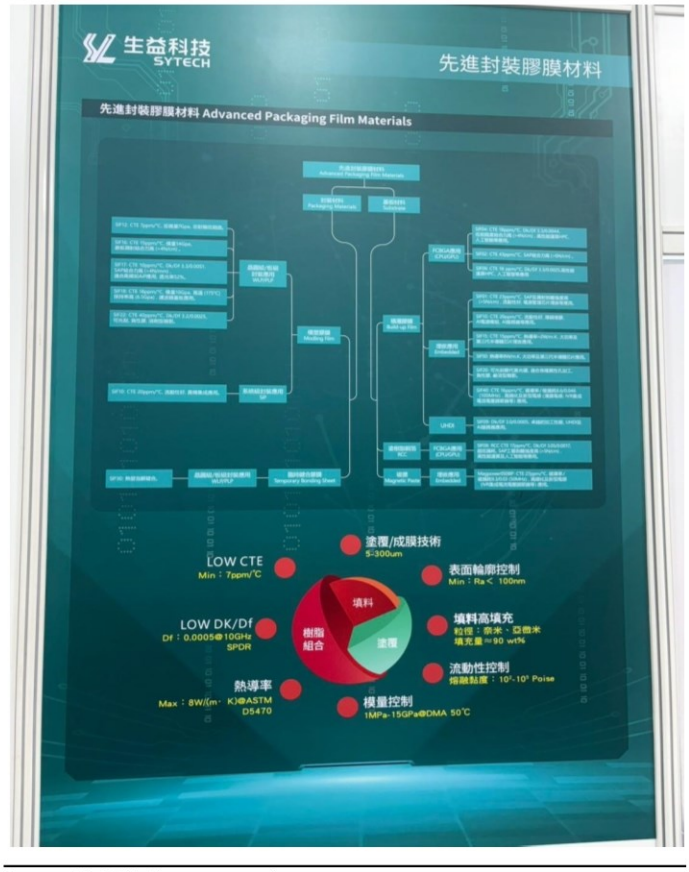
Fig. 31: EMC's substrate CCL roadmap



	Property	Condition	Unit	EM-S526	EM-S536K	EM-S570	EM-S570T	EM-S572T
Thermal	Tg	DMA	℃	260	260	320	320	320
	X/Y CTE	<Tg, TMA	ppm/℃	9/10	7/8	4/6	2/3	0.8
	Z CTE	<Tg, TMA	ppm/℃	25~30	15~20	8~13	5~10	4~8
Mechanical	Modulus	R.T.	Gpa	26	24	32	37	40
	Peel Strength	12μm VLP	kgf/cm	0.9	0.7	0.9	0.9	0.9
Electrical	Dk	10GHz (RC 70%)	-	3.4	3.0	3.8	3.7	3.75
	Df		‰	7.6	1.8	7.4	8.5	7.3

Source: EMC, Nomura research

Fig. 32: SYTECH's substrate build-up film offerings



Source: SYTECH, Nomura research

Fig. 33: WAZAM's CBF roadmap



Source: Wazam, Nomura research

PCB/HDI

AI PCB/CCL project updates: – 2H27F trending to M9K1/K2 with more HDI structures

As shown in *Fig. 34* , given the rising GPU/ASIC performance and lower signal loss requirements in the next-gen AI server platforms, we expect new AI GPU/ASIC platforms to increasingly adopt M9K1/K2 CCL (mixed with M4/M6) as mainstream in 2H27-2028F, vs the current generation M8K1/K2 mixed with M4/M6, while the PCB structure will move from high layer count (HLC), M+N, to more high density interconnect (HDI; HDI+3-6) or HDI mixed with M+N structure. It's widely expected that nVidia will stick with HDI+5 for its compute boards for Rubin Ultra. We believe more ASIC or non-nVidia GPUs will adopt near-package optics (NPO) for scale-up/out, and this will also accelerate the adoption of high layer count HDI for switches and compute boards. We do not see broadening adoption of Q glass aside from the existing Rubin HGX UBB and LPU in 2027F, likely due to the difficulty of PCB processes and the availability of M10 resin. We are still waiting to see if PTFE+HCR or HCR+HCR will be adopted in Rubin Ultra's new switch boards in 2H27F, and it will not be confirmed this early. We see EMC is still the major CCL supplier across all major AI platforms, and Nanya is emerging as a newcomer at a time when end-customers are looking for alternative suppliers, given the tight supply in all the high-end CCL providers. We believe the migration to HDI trend is positive for VGT, ZDT, Unimicron, and WUS, while most HLC PCB producers are trying to enhance their HDI capabilities.

Fig. 34: A summary of AI PCB/CCL specs and supply chain

nVidia

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
H100	OAM	2H23-1Q25	5+8+5 HDI (18L)	M7	EMC	Unimicron (major), VGT, others
	UBB		24L PCB	M7	EMC	WUS, ISU, TTM, others
B200	OAM	2H24~	5+10+5 HDI (20L)	M8+M4	Doosan	Unimicron, VGT, others
	UBB		18L PCB	M7+M4	Doosan	WUS, ISU, TTM, others
B300	OAM	2H25~	5+10+5 HDI (20L)	M8+M4	Doosan	Unimicron, VGT, others
	UBB		22L PCB	M8+M4	Doosan	WUS, ISU, TTM, others
GB200 (Bianca)	Bianca board	2H24~	5+12+5 HDI (22L)	M8 (HVLP3)+M4	Doosan	VGT (major), Unimicron, others
	Switch tray	2H24~	6+12+6 HDI (24L) 22L PCB	M7 (HVLP2)+M2 M8/8.5 (HVLP2) hybrid	EMC EMC, SYTECH	WUS (major), VGT, Unimicron, TTM?, others
GB300 (Bianca)	Bianca board	2Q25~	5+12+5 HDI (22L)	M8 (HVLP3)+M4	Doosan	VGT (major), Unimicron, others
	Switch tray	2Q25~	22L PCB	M8/8.5 (HVLP2) hybrid	EMC, SYTECH, Doosan	WUS (major), VGT, Unimicron, TTM, others
VR200 (Bianca)	Strata board	2Q26~	5+16+5 HDI (26L)	M8 (HVLP4)+M4	Doosan	Unimicron (major), VGT(major), ZDT(emerging), others?
	Mid-plane boards in trays	2Q26~	44L PCB	M9K2	EMC, SYTECH	VGT, WUS, Kinwong
	Switch tray	2Q26~	32L PCB	M8.5 (K2, HVLP4)	EMC, SYTECH	VGT, Kinwong, WUS, TTM, others?
V200 HGX	UBB	2H26	?	M9Q+M8K2	EMC	VGT?
Vera server	Compute board	Late-2026?	5+14+5 HDI (24L)	M7 (HVLP3)+M4	Doosan	VGT, Unimicron, others?
LPU	Compute board	1Q27?	48L?	M9Q+M8K2	EMC	Kinwong, VGT, WUS, others?
Rubin Ultra	Strata board	3Q27~?	5+18/20+5 HDI (28/30L)?	M9K1 (HVLP4)+M4?	Doosan	Unimicron (major), VGT(major), ZDT(emerging), others?
	Mid-plane boards in trays	3Q27~?	? 44L?	? M9Q?	EMC, SYTECH	VGT, WUS, Kinwong?
	Switch tray	3Q27~?	M9Q? PTFE+HC? HC+HC? 32L?	M9Q? M10Q? PTFE+HC? HC+HC? M8(K2)/M9+PTFE?	EMC, SYTECH? Taiflex?	VGT, Kinwong, WUS, Flexium?, SCC?, TTM??
Feynman	Backplane?	2H28?	156L PCB (26x6)?	PTFE+PTFE? PTFE+HC?	SYTECH? Taiflex? Others?	Kinwong?, VGT? WUS?

AWS

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
Trainium 2	OAM	2H24~4Q25	HDI+3	M6? (HVLP2, RTF)	Panasonic	Shengyi
	UBB		26L PCB (2 ASICs per board, air cool)	M8 (HVLP2)	EMC, TUC (starting from June 2025)	GCE, Shengyi, FHE
Trainium 2.5 & 3 (air cooled)	OAM		HDI+4 (22L)	M6?M7? (HVLP2, RTF)	EMC?	Shengyi, ZDT
	UBB	Trn2.5: 1Q26~ Trn3: 2Q26~	26L PCB (2 ASICs/tray - air-cooled)	M8 (HVLP4)	EMC, TUC	GCE, Shengyi, FHE,
	PDS switch	2Q26~	22L/26L HLC PCB	M8+M4	EMC	WUS, Shengyi, ZDT, GCE? FHE?
Trainium 3.5? 4? (liquid-cooled)	Compute board	4Q26 (Trn3.5)? 4Q27 (Trn4)?	3+28+3 HDI (34L) (4 ASICs/tray - liquid-cooled)	M9K2 (HVLP3?)+M4?	EMC, NY?	GCE, ZDT, Shengyi?

Google

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
TPU 7x	TPU UBB	2H25~	34L PCB (16+18, N+M)	M7, HVLP2	Panasonic, EMC	WUS, ISU, TTM, VGT
	CPU board (New) - x86 CPU	4Q25~	16-18L	M6	Panasonic	WUS, TTM, GCE?
TPU 8t, 8i	TPU UBB	mid-26~	34/36L PCB	M8K2+M7, HVLP3	Panasonic, EMC	WUS, ISU, LCS, GCE?
	CPU board - Axion	3Q26~	22L PCB	M6.5	EMC, Panasonic, NY?	VGT, WUS, ISU, TTM, others?
	8t/i all-to-all switch	4Q26?	22L PCB	M8?	EMC	GCE, VGT, ZDT, others?
TPU 9	TPU UBB?	2028?	HDI+6?	M9K2+M6/7? HVLP4/3?	Panasonic? EMC?	WUS, ISU, Unimicron, VGT, ZDT?
	CPU - Madeline Beach	End-27?	?	M6.5? M7?	EMC, Panasonic, NY?	VGT? Tripod?
	More other boards?					

Meta

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
Athena	OAM, UBB	2Q26?	36L+?	M8+M4	EMC	WUS, ISU, TTM
Iris	OAM, UBB	2H26~	40L+?	M8+M4	EMC	WUS, ISU, TTM

AMD

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
MI450	UBB	2H26~	48L HDI+HLC PCB (26+22, HDI+3)	M8K1+M4? M8K1?	EMC, Doosan	SCC, Daeduck, others?
	Networking	2H26~	18~26L HLC	M8K1+M7?	EMC, Doosan?	SCC, WUS, Daeduck, others?
MI550	UBB	2H27?	HDI+2 mixed with M+N	M8K1+M7? M8K1?	EMC, Doosan	SCC, Daeduck, Dynamic, others?
	Networking	2H27?	?	??	EMC, Doosan?	SCC, WUS, Daeduck, others?

Microsoft

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
Cobalt 300	CPU board	3Q27?	24L?	M7+M4	EMC	WUS, ISU, GCE?
Maia 300	?	2H27?	40L (N+M)?	M8K2?+M6?	EMC?	WUS, GCE, TTM?

Source: Company data, Nomura estimates

Fig. 35: CCL material migration

Halogen-free

Ethernet protocol	100GbE x 64 (28Gbps)	400GbE x 32 or 64 (56Gbps)	800GbE x 64 (112Gbps)	1.6TbE (224Gbps)	3.2TbE (448Gbps)
PCIe protocol	PCIe 5.0 (32GT/s)	PCIe 6.0 (64GT/s)	PCIe 7.0 (128GT/s)	PCIe 8.0 (256GT/s) and above	
CCL	**M6 Very Low Loss**	**M7 Ultra Low Loss**	**M8/M8.5 Extreme Low Loss**	**M9 Supreme Low Loss**	**M10/M11 Supreme Low Loss?**
EMC (Dk/Df)	EM-891 (3.2/.45)	EM-890K (2.8/.24)	EM-892K2 (2.8/.13)	EM-896K3 (2.7/.07)	EM-898K4 (3.1/.04)
	EM-528 (3.5/.58)	EM-626K (2.9/.25)	EM-892K (2.8/.17)	EM-896K2 (2.8/.09)	
		EM-891K (3.0/.33)	EM-628K (2.8/.17)		
		EM-890 (3.0/.36)			
		EM-626 (3.1/.38)			
TUC (Dk/Df)	TU-901 (3.59/.36)	TU-933+ (3.08/.20)	TU-943HR (3.14/.11)	TU-953Q (2.99/.066)	TU-973Q (2.7/.035) (PTFE)
	TU-885 (3.43/.31)	TU-901N (3.30/.18)	TU-943SR (3.16/.13)	TU-953R (3.19/.08)	TU-973F (2.7/.020) (PTFE)
	TU-883A (3.44/.32)	TU-901Q (3.07/.14)	TU-902R (3.19/.107)		TU-963Q (2.95/.040)
	TU-883C (3.39/.45)	TU-885 Sp (3.15/.17)	TU-953N (3.20/.11)		TU-963F (2.85/.036)
		TU-883A Sp (3.17/.18)	TU-943HN (3.16/.13)		
			TU-943SN (3.16/.14)		
			TU-902N (3.20/.12)		
ITEQ (Dk/Df)	IT-968G (3.59/.50)	IT-988GLSE (3.34/.26)	IT-998GSE2 (3.16/.13)	IT-999GSE3 (3.03/.07)	IT-Q10GSE4 (2.9/.04) (PTFE)
	IT-602G (3.50/.60)	IT-968GSE (3.16/.36)	IT-998GSE (3.45/.17)	IT-999GSE2 (3.12/.09)	
		IT-988GL (3.63/.41)			
Doosan (Dk/Df)	DS-7409DJG (3.30/.37)	DS-7409DJG(N) (3.00/.20)	DS-7409DQN2 (2.69/.11)	DS-7409DCQ (2.90/.10)	DS-7409DZQ (?/.04)
	DS-7409DV(T) (3.30/.45)	DS-7409DV(NT) (3.10/.37)	DS-7409DQN (3.20/.17)	DS-7409DYQ (2.90/.10)	
				DS-7409DCN2 (3.00/.13)	
				DS-7409DYN2 (3.00/.13)	
				DS-7409DCN (3.10/.15)	
				DS-7409DYN (3.10/.15)	
Panasonic (Dk/Df)	R-537Y(N) (3.36/.29)	R-578Y(GN) (3.31/.23)	R-579YS(U) (3.19/.12)	R-5797Q (3.0/.07)	
	R-5775(N) (3.35/.40)	R-5785(GN) (3.35/.20)	R-579Y(U) (3.08/.12)	Megtron 9? (3.2/.10)	
	R-537Y(E) (3.66/.37)	R-578Y(N) (3.31/.23)	R-579YS(N) (3.22/.15)	Megtron 9? (3.2/.12)	
	R-5775(K) (3.62/.46)	R-5785(N) (3.40/.20)	R-579Y(N) (3.13/.16)		
	R-5775(G) (3.62/.46)	R-578Y(GE) (3.60/.34)			
		R-5785(GE) (3.61/.30)			
SYTECH (Dk/Df)	Synamic 8GX (?/.33)	Synamic 8GN (3.28/.19)	Synamic 9GN2 (?/ .11)	Synamic 10GQ (3.15/.06)	SG5300N (PTFE)
	Synamic 6G (?/.33)	Synamic 8NE (?/.17)	Synamic 9N2 (?/.12)	Synamic 10GN2 (?/.09)	Synamic 11GQ (?/.04)
	Synamic 6GX (3.73/.50)	Synamic 6N (3.35/ .21)	Synamic 9NH (?/.12)		
	Synamic 6 (3.68/.36)		Synamic 9NX (?/.14)		
	Synamic 8G (3.66/.32)		Synamic 9GN (3.34/ .14)		
			Synamic 9N (?/ .14)		
Nanya (Dk/Df)	NPG-188U (3.54/.34)	NPG-199 (3.58/.32)	NPG-199HK (3.24/.14)	NPG-999Q (3.00/.045)	NPG-A99 (2.8/.035)
	NPG-188H (3.60/.36)		NPG-199K (3.26/.16)	NPG-999K2 (3.06/.07)	
				NPG-999K (3.18/.083)	
Isola (Dk/Df)	I-Tera MT40 (3.45/.31)	Tachyon 100G (3.02/.21)	TerraGreen 400G2 (3.10/.15)	Tachyon 200JV (?)	
	IS580G (3.80/.60)	TerraGreen 400GE (3.29/.26)	TerraGreen 400G (3.15/.17)		
Ventec (Dk/Df)	VT-462SH NF/LF (3.2/.40)	VT-770(LK) (3.3-3.4/.24)	VT-772+(LK2) (2.9/.13)	VT-468(Q) (2.5/.05)	
	VT-462S (3.5/.50)	VT-770 (3.4-3.5/.40)	VT-772+(LK) (3.1/.17)	VT-468(LK2) (3.1/.09)	
NOUYA (Dk/Df)	NY6666SE (3.75/.37)	NY6666N (3.5/.20)	NY8888N2 (3.17/.12)	NY-P5Q (3.1/.07)	
	NY6300S (3.9/.40)	NY6300SN (3.45/.25)	NY8888N (3.17/.14)	NY9999Q (3.15/.07)	
	NY6300SL (4.20/.51)	NY6666 (3.9/.38)	NY-P4N (3.22/.14)		
	NY6300 (3.95/.42)	NY-P3 (3.4/.22)	NY-P4 (3.2/.115)		
	NY-P1 (3.9/.40)	NY-P2 (3.5/.25)			

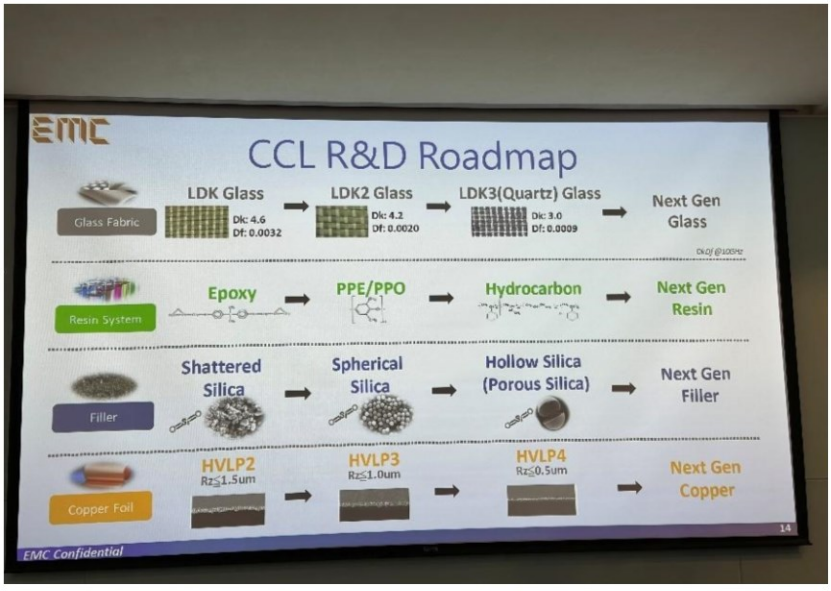
Copper foil	**HVLP (A-)RTF**	**HVLP2 (A-)RTF2**	**HVLP3 (A-)RTF3**	**HVLP4/4+ (A-)RTF4**	**HVLP5 (A-)RTF5**
Mitsui (Rz, um)	HS1-VSP (1.5)	HS2-VSP (1.0)	SI-VSP (0.6)	SI2-VSP (0.5)	SI3-VSP (0.5)
	MLS-G (2.5)	MLS-G3 (1.5)	MLS-G4 (1.2)	MLS-G5 (1.2)	
Furukawa (Rz, um)	FV-WS (1.2)	FZ-WS (1.0)	F1N-WS (0.9)	F0X-WS (0.8)	FPR-WS
	DGTSEU2-MP (3.0)	DX1-MP (2.0)			
Fukuda (Rz, um)	T9FB-SV	T9S-SV	DSV-A	T9DA-SV (0.85; Japan)	T9DC-SV (Suzhou)?
	TGFB-DSTF(M)	T9-DS2	T9-DS3	T9-DS4	
Circuit Foil (Rz, um)	BF-TZA (2.5)	BF-ANP (1.2)	BF-NN (1.0)	BFL-NN/BFL-NX (0.6)	BFL-NF (0.6)
	TZA-B (4.2)	TZA-B2 (2.5)	TZA-B3 (2.1)	TZA-B4 (?)	
Co-tech (Rz, um)	VL410 (2.0)	VG410 (1.5)	VL411 (0.7)	PF51N (0.5)	PF511 (0.45)
	RT311 (3.0)	RG311 (2.1)	RG312 (1.8)	RG313+ (1.0)	RG315?
Nanya (Rz, um)	TLCV2 (2.1)	TLCV1 (1.5)	V1A (1.0)	VZA (0.75)	VNC (0.45)
	TLCHP (2.5)	H1/H1V (1.5)	H1A (1.2)		
Defu (Rz, um)	V-HS1 (2.0)	V-HS2 (1.5)	V-HS3 (0.8)	V-HS4 (0.8)	V-HS5 (?)
	RHS1 (3.0)	RHS2 (2.3)	RHS3 (2.1)	RHS4 (1.9)	RHS5 (?)
Chang Chun (Rz, um)	VFP-111 (0.86)	VFP-101 (?)	VFP-200 (0.73)	VFP-250 (0.26)	VFP-300 (0.26)
	RTF (3.5)	RTF-25 (2.1)	RTF-35 (2.01)	RTF-45 (1.47)	RTF-55 (?)
Huanergy (Rz, um)	HVP11 (2.0)	HVP21 (1.5)	HVP31 (1.0)	HVP41 (0.8)	HVP51 (0.6)
	HRO21/HRP21 (4.0)	HRO31/HRP31 (2.3)	HRP41 (2.1)	HRP51 (1.7)	

Glass fiber cloth	**E Glass**	**NE/Low Dk Glass**	**NER/Low Dk 2 Glass**	**NEZ Glass**	**Q Glass**
Dk @10GHz	6.6	4.7	4.5	4.0	3.4
Df @10GHz	0.006	0.0025	0.0018	0.0010	0.0004
CTE (ppm/°C)	5.6	3.3	3.4	3.1	0.5-0.6

Note: (1) For M7 and above, the name (e.g., ultra-low loss, extreme-low loss) can vary across different companies. (2) For CCL, Df is measured in %; Dk/Df @10GHz, except for some of Panasonic's parts (@12/13/14GHz). (3) The specs of RTF copper foil are not comparable to HVLP. We put the two types of copper foil in parallel for development illustrative purposes only.

Source: Company data, Nomura research

Fig. 36: CCL R&D roadmap



Source: EMC, Nomura research

Copper foil shortage in the making?

While copper foil supply does not seem to be an issue in 2026, we learn from CCL vendors that supply could become tighter in coming quarters, across high tiers, driven by ramp-up of new AI platforms, and low tiers, driven by a reduced industry supply. For high-end copper foil (HVLP4; hyper very low profile), Co-tech (8358 TT, Not rated) talked about strong customer queries for HVLP4+ and plans **10,000 tons of HVLP3/4+ capacity addition p.a. in 2027-29E (primarily HVLP4+) in Taiwan and Malaysia**. If everything progresses as planned, Co-tech expects to acquire a land in Malaysia and complete the plant layout for construction kick-off in 1Q27 and completion by end-2028. Meanwhile, Co-tech officially terminated production of low-end high-temperature elongation (HTE)/reverse treated foil (RTF) from September and would convert the lines in Plant 1 and Plant 2 to RG (advanced RTF)/HVLP production. The company expects a tighter HVLP supply status into 2028-29E and is mulling over increasing treatment fees given more complicated processing. Capacity conversion of leading copper foil makers might also lead to **low-end copper foil supply crunch** in the making, and we notice some low-grade CCL vendors could look to introduce more Chinese suppliers like Defu, Tongguan, and Huanergy (unlisted).

In terms of technological advancement, Co-tech expects to sample HVLP5 by end-2026E, for potential adoption in M9/M10 grade CCL. Mitsui Kinzoku (5706 JP, Buy) displayed **FaradFlex** that incorporates decoupling capacitors into copper foil to reduce board thickness, impedance, and electromagnetic interference (EMI) noise, while improving signal integrity. Our Japan analyst Kaori Iwasaki recently also wrote about increased use of FaradFlex in AI server switches (*report*).

Fig. 37: HVLP production capacity (t/month)

Company	Production site(s)	HVLP production capacity (t/month)									Current status
		2023	2024	2025	2026E	2027E	2028E	2029E	2030E	2031E	2032E	
Mitsui Kinzoku	Taiwan Malaysia	420	420	620	840	1,000	1,200	1,200	1,400	2,000	2,600	1) Will expand to 1,200t/month in 2028E (860t/month in Taiwan and 340t/month in Malaysia). 2) Mitsui Kinzoku can increase capacity to 5,000t/month at the second plant in Malaysia, which it plans to acquire.
Furukawa (23/4 = 100)	Japan (Tochigi) Taiwan	100	200	310	465	465+	465+	465+	465+	465+	465+	Produces HVLP1-4.
Co-tech	Taiwan Malaysia (planning)	100	100	208	333	833	1,667	2,500	2,500+	2,500+	2,500+	Expanding HVLP3/4 capacity through conversion and a new factory build.
Defu	China (Jiujiang, Jiangxi)	?	?	250	575	2,275	3,000+	3,000+	3,000+	3,000+	3,000+	1) Defu's annual PCB copper foil capacity in China is about 50kt, which could be converted to HVLP, according to the company. 2) Defu announced to invest CNY1bn in domestic PCB copper foil capacity.
Circuit Foil	Luxembourg	?	?	567	567	567	567	567	567	567	567	Circuit Foil has an annual capacity of 16.8kt, of which 6.8kt is for HVLP4.
Lotte Energy Materials	South Korea	?	?	308	558	1,333	1,667?	1,667?	1,667?	1,667?	1,667?	1) Lotte Energy Materials plans to increase the circuit foil production capacity at its Iksan plant in Korea from 3,700t/year in 2025 to 6,700t/year in 2026, and to 16kt/year in 1H27. 2) It is considering additional capacity in 2028 and beyond, and is ultimately aiming for annual output of 20,000t.
Fukuda Metal Foil & Powder	Japan (Kyoto)	?	?	?	300?	300?	300?	300?	300?	300?	300?	
Tongguan	China (Chizhou, Anhui)	?	?	?	250	250+	250+	250+	250+	250+	250+	1) Tongguan has 55kt of annual PCB copper foil capacity, and plans to convert 3000t/year to HVLP. 2) Can produce HVLP1-4. It is currently ramping up HVLP4.
Long Young/GHZ Foil	China (Huaian, Jiangsu)	?	?	?	?	?	?	?	?	?	?	Mostly sampling volume; still no track record in the high-end market.

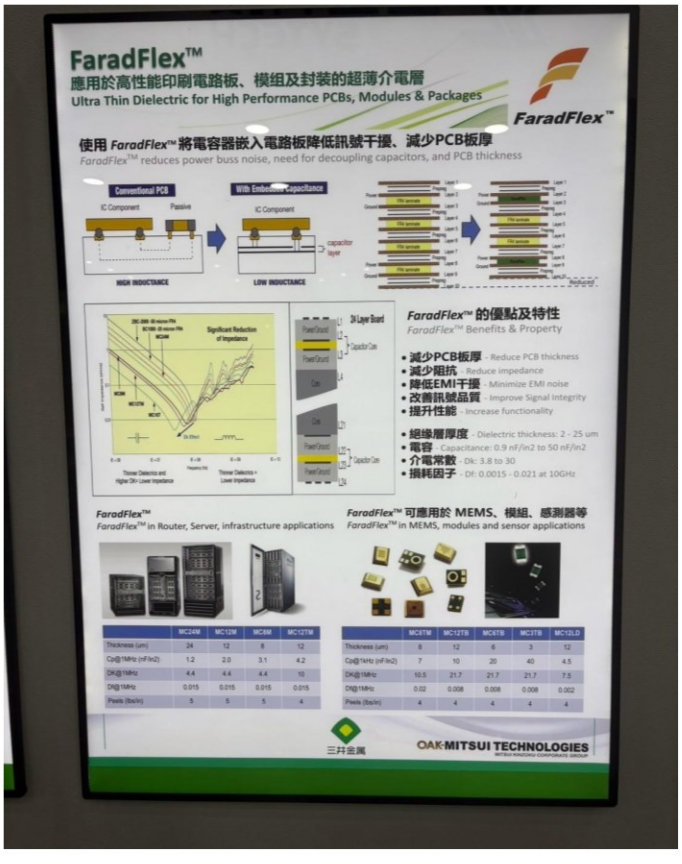
Note: Furukawa Electric does not disclose production capacity. Rebased so that April 2023 = 100, based on materials from the business briefing on 4 June 2025. At the briefing on 4 June 2026, the company said it plans to increase production capacity by 50% in 27/3 Q4.
Source: Company data, Nomura research

Fig. 38: Co-tech's copper foil technology roadmap



Source: Co-tech, Nomura research

Fig. 39: Mitsui Kinzoku's FaradFlex

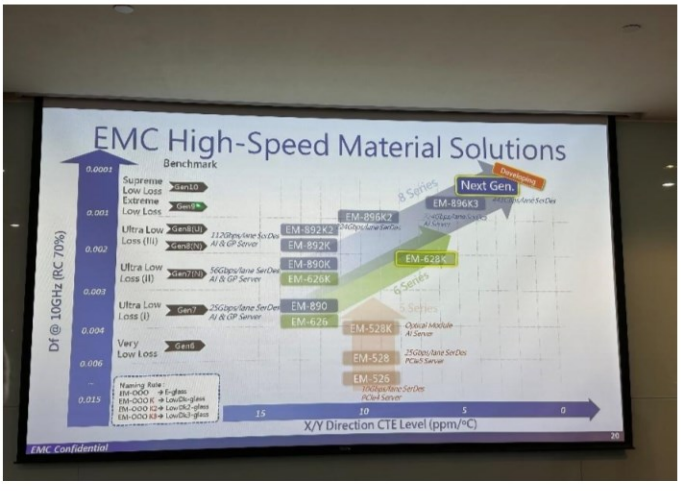


Source: Mitsui Kinzoku, Nomura research

Resin could dictate upcoming laminate development routes

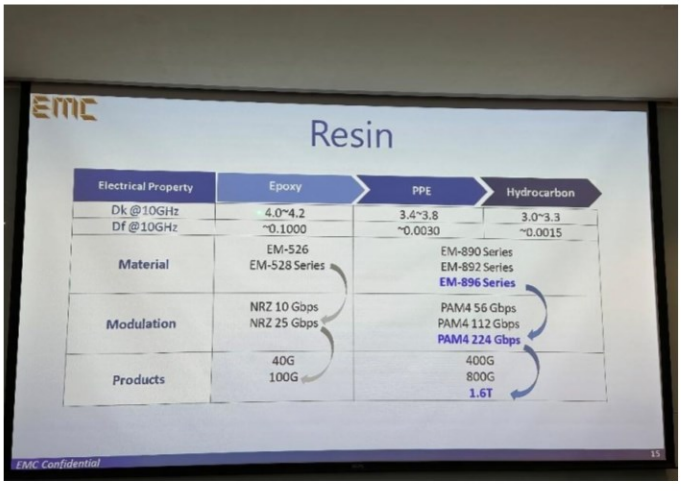
We believe polymerization in the resin system for better electric performance (lower dielectric constant [Dk] is an option for CCL makers to drive material upgrades, and they might work on either **pushing the envelope of hydrocarbon resin (HCR) or exploring any approach to improve the intrinsically poor processability of thermoplastic polytetrafluoroethylene** (PTFE; more details in the following paragraphs). EMC, Doosan, and Nanya appear to stay in the HCR camp by polishing the resin recipes and additives; SYTECH and TUC each has introduced PTFE to their roadmap beyond M9/M10. We believe EMC could see rising contribution of M9 CCL in 2027F as new AI platforms could move from EM-892 series (M8) to EM-896 series backed by resin upgrades, whereas the incorporated fiber cloth could be low-Dk 2 glass (K2) or Q glass (K3/K4).

Fig. 40: EMC's high-speed material solutions



Source: EMC, Nomura research

Fig. 41: EMC's resin upgrades



Source: EMC, Nomura research

More attention on filler

Raw material development for CCL requires holistic evaluation, and the importance of filler in the laminate is increasing. One common debate between HCR and PTFE is the higher Dk of HCR vs intrinsic softness of PTFE, and we believe CCL makers might look to **reduce the Dk of HCR or increase the mechanical strength of PTFE** by blending fillers into the resin:

- Adding **hollow fillers** could lower the Dk of HCR due to the lowest relative permittivity of air, but hollow inorganic fillers could make the resin compound more fragile, according to companies. Mixture homogeneity is also a concern.
- Adding **silica filler** to PTFE could boost the rigidity due to a lower CTE of silicon dioxide, but a higher Dk of silica could hinder the excellent electrical properties of PTFE, according to companies.

Sekisui Kasei (4228 JP, Not rated) demonstrated its TECHPOLYMER organic filler for resin. The standard TECHPOLYMER has hollow particle offerings to improve the electrical performance of resin, and organic polymer carries better intrinsic toughness than inorganic filler during the blending process. The soft-grade TECHPOLYMER, on the other hand, is a new low-dielectric grade lineup with enhanced flexibility to help relieve internal stress within materials and thus suppress board warpage and cracking caused by the increasing size of PCB. However, the temperature tolerance of organic materials is naturally lower (around 300°C for TECHPOLYMER) and thus unable to support PTFE.

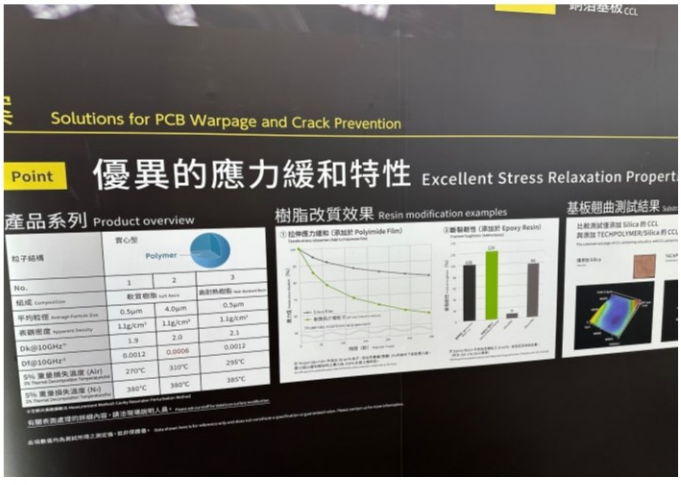
Interestingly, Sekisui Kasei flagged that **organic and inorganic fillers** could be complementary. By combining its TECHPOLYMER hollow particles with **Denka**'s (4061 JP, Buy) low-dielectric silica in HCR, the composite could capture the benefits of each material (i.e., lower CTE by silica and lower Dk by TECHPOLYMER).

Fig. 42: Standard TECHPOLYMER organic filler



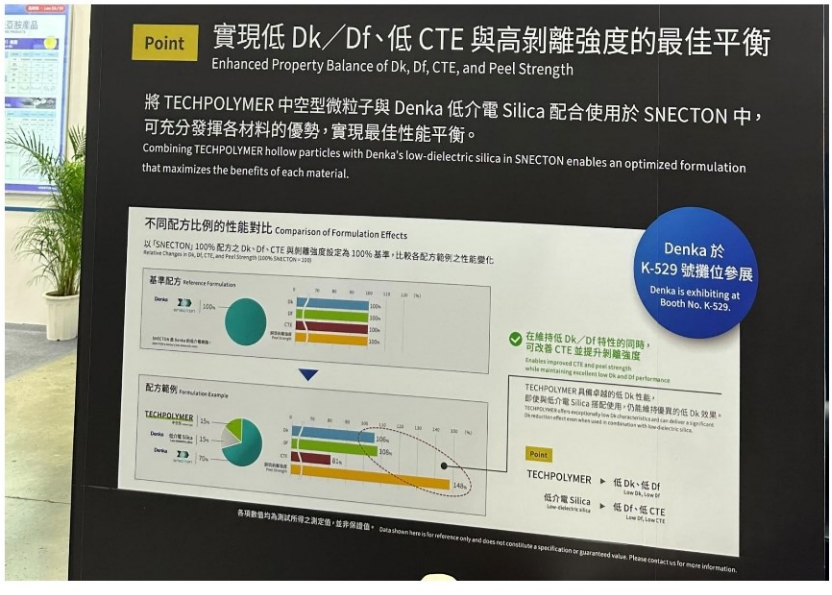
Source: Sekisui Kasei, Nomura research

Fig. 43: Soft-grade TECHPOLYMER organic filler



Source: Sekisui Kasei, Nomura research

Fig. 44: A combination of organic and inorganic filler to lower Dk and CTE



Source: Sekisui Kasei, Nomura research

The development progress of PTFE is worth monitoring

nVidia's display of an NVLink PTFE board at the OCP Global Summit reignited industry discussions about the feasibility of PTFE adoption in HLC PCB, somewhat echoing *our feedback* from the booth tour last year that the supply chain was dedicated toward improving PTFE processing such that PTFE might emerge as a candidate to support subsequent upgrades beyond M10.

TUC noted substantial differences in Dk and dissipation factor (Df) between fiber cloth and resin. Based on the experiment, stacking up core laminate and prepreg (both without fiber cloth) of symmetric Dk could hold the composite Dk within tolerance balance, but the addition of fiber cloth to prepreg (Q glass in this study) could result in signal degradation (skew and resonance) at high frequency.

TUC further elaborated on the resin system:

- PTFE has a lower Dk, but the curing temperature is 380°C (vs. regular press machine running at 220°C) at curing time >6 hours with high lamination pressure (~600psi).
- HCR processing needs a lower curing temperature (<250°C) and cycle time (<3 hours), but the Dk is higher.

A hybrid system (PTFE+HCR) is one of the approaches to balance the advantages of of

PTFE and HCR, and yet there are several inherent PCB processing problems for pure/hybrid PTFE systems to consider, with and without fiber cloth: 1) hybrid curing/lamination; 2) desmear; 3) drilling; 4) interface bonding; 5) dimension stability and registration; and 6) HDI/sequential lamination designs. TUC presented four sets of stack-up solutions for PCB makers to decide on **signal integrity priority, process priority, or reliability priority**, and suggests **either core or prepreg should incorporate fiber cloth for CTE reliability consideration** (TUC's solution uses Q glass).

Fig. 45: Pros and cons – PTFE and HC hybrid design

Key challenges in PCB applications Core PP	PTFE w/o glass PTFE w/o glass	PTFE w/o glass HC with glass	PTFE with glass PTFE with glass	PTFE with glass HC w/o glass	PTFE with glass PTFE w/o glass	HC with glass HC with glass
SI performance (ranking)	1	2	1	2	1	3
CTE (ranking) X/Y/Z	3	2	1	3	2	1
Signal skew effect@high frequency	1	2	3	2	1	3
Interfacial bonding (resin-glass fiber)	N/A	NA/Good	Weak/Weak	Weak/Good	Weak/NA	Good/Good
Interfacial bonding (resin-resin) core/PP	Medium	Weak	Medium	Weak	Medium	Good
CAF risk	N/A	Low	Medium-High	Medium	Medium-High	Low
Warpage during PCB reflow process	High	Medium-High	Low-Medium	Medium	Medium	Low
Mechanical strength	Weak	Medium	Weak-Medium	Medium	Weak-Medium	Good
Adaptability to complicated circuit design	Weak	Medium-High	Weak	Medium	Weak	Good
Difficulty in drilling process	Medium-High	Medium	Medium-High	Medium	Medium-High	Low
Difficulty in desmear process	High	Medium	High	Medium	High	Low-Medium
Overall weighting/feasibility	X	X	?	V	?	V

Source: TUC, Nomura research

Fig. 46: TUC's M10/M11 solutions

Solution	Core	PP	Resin system	Loss level @26.56GHz
SI priority	TU-973Q	TU-973F	PTFE	0.37-0.40
SI & process priority	TU-973F	TU-963Q	PTFE+HCR	0.40-0.43
SI & process priority	TU-973Q	TU-963F	PTFE+HCR	0.40-0.43
Reliability priority	TU-963Q	TU-963F	HCR	0.43-0.47

Source: Company data, Nomura research

We interacted with some PTFE board makers as well. They shared that the electrical performance difference between HCR and hybrid PTFE is not particularly significant, but their material suppliers are promoting hybrid PTFE and do not offer pure HCR solutions. For a cloth-free solution, thermal expansion stability is extremely difficult to control, and only nVidia is pursuing this approach.

As per their feedback, equipment requirements are also broadly similar with conventional PCB/CCL manufacturing process, with key differences lying in the lamination and desmear tools. Initial drilling for PTFE with CO_2 lasers leaves residue at the bottom of vias, requiring additional UV laser processing. High-temperature lamination equipment, supplied by **JSW** (5631 JP, Not rated), **Bürkle** (unlisted), and **Indubond** (unlisted), is not a necessity but could make production parameter adjustments easier.

Backlogs might prolong the equipment lead time

The aforementioned **Mitsubishi Electric's CO_2 laser drilling** machine lead time is currently three years, since the tool is shared by laser vias for both ABF substrates and HDI, which are both undergoing capacity expansion. Incumbent HDI manufacturers like Victory Giant, ZDT and Compeq are looking to expand their capacity, along with some potential new entrants from HLC, due to the fact that HDI could support higher I/O routing density. Our observations also indicate more adoption of HDI in the mainboards for new AI platforms in 2H27-1H28F.

Ta Liang (3167 TT, Not rated) showcased its metrology tool **"TM4"** for stub depth control during the exhibition that features four spindles with faster via probing for higher throughput than prior TM3 (single spindle). While PCB makers may purchase TM3 for sampling purposes, Ta Liang believes TM4 is a better option for production runs, and one unit TM4 can pair with five units six-spindle back-drillers in general. The company is confident that TM series can enable **stub length at ±2mil** which is a critical parameter for NVLink switch boards, and has no plan to sell TM series on a standalone basis.

Ta Liang sees driller/router tool demand visibility through 2027E given PCB makers' capacity expansion plans. **It currently manages >400 units/month of equipment capacity plus 50 units/month of outsourced capacity, and expects to expand to**

>600 units/month by 2Q27E plus 150 units/month of outsourced production. Ta Liang's current equipment **lead time is about six months**, but management highlighted the delivery pattern could be staggered subject to customers' new plant build-out progress. A few PCB makers are increasing purchases of Ta Liang's drillers/routers given unsatisfying delivery by competitors like Schmoll (unlisted), based on the company's observations.

We also visited **MKS** (MKSI US, Not rated), a leading horizontal plating equipment maker for HDI and multi-layer boards. According to management, current lead time to shipment is six months on average, and given robust demand, MKS is adding one more factory in Guangzhou, scheduled for operations from 3Q27E to double the output of its existing capacity in Guangzhou (mostly PCB plating tools). In the meantime, it works on expansion in the Germany factory for more module production to support Asian customers.

ESI (unlisted), the UV laser drill system arm of MKS, has been a dominant UV laser driller provider for flexible PCB (FPC) which is subject to handset demand cyclicality. Interestingly, we learned from our visit that ESI's UV laser is also gaining traction in antenna rigid boards given different hole size requirements. Management observed rising order momentum recently for their PCB laser tools thanks to surging demand for satellite ground terminals.

Lamination press availability could be a constraint, with **high-temperature lamination press** suppliers' capacity fully booked even without PTFE PCB/CCL orders (right now only a few shipments for R&D). Limited productivity makes lead times extend from 10 months (Indubond) to 2 years (Bürkle) due to strong demand from PCB, substrate cores and probe cards. Conventional thermal oil laminator requires continuous boiler heating, which carries an explosion risk, whereas Indubond's induction bonder eliminates the need for oil boilers and offers a much smaller footprint of only around 1.2x1.3m. Indubond's equipment allows users to stack chambers up to four-chamber height to save floorspace. A complete lamination press cycle is around 5-6 hours.

Optical module board

We visited **ZDT and Compeq** and learned the latest optical module board trends.

As shown in *Fig. 47*, **2.5D CPO**, in which OEs are placed on top of switch substrate surrounding the switch IC, the OE module may or may not use IC substrate/mSAP (modified semi-additive process) board, depending on the OE is socketed or solder bonded.

NPO requires at least 16-18L mSAP HDI board, vs **12-16L mSAP for 1.6T pluggable and 10-12L mSAP for 800G pluggable optical module**. Some initial designs for NPO were 22L+mSAP, but now are optimized to 16-18L (most likely 18L is mainstream). It looks difficult to further lower the layer count of NPO boards, in our view. **NPO doesn't require gold finger process**, as it is not a pluggable type.

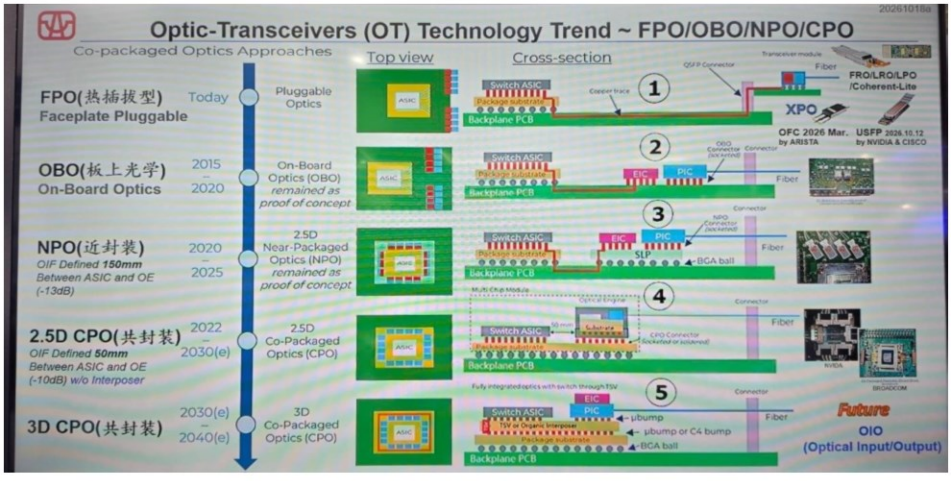
USFP is the latest standard (single lane 400G) for pluggable optical modules, developed by nVidia and Cisco (CSCO US, Not rated), while the technology will need to wait for 400G/lane EML or silicon photonics (SiPh)+thin film lithium niobate (TFLN) to commercialize. It will be used for 6.4T and 12.8T, and may drive higher content for mSAP board.

Embedded silicon capacitor (Si-cap) is a trend in optical module boards, which can resolve the insufficient surface issue for increased components in future products and can let high-frequency capacitors (e.g., Si-cap) process high frequency signals. For example, each NPO mSAP can embed 10-50 units of Si-caps. ZDT has been familiar with embedded technologies in mSAP/PCBs, which demonstrate in its track record in embedding active ICs (not only passive components) inside mSAP for AirPods for years.

Optical module boards do not need PTFE or Q-glass, as the transmission distance inside the optical transceiver is very short. Module makers tend to overcome any signal loss issue through optical design changes, rather than using PTFE or Q glass, which are very difficult to process in HDI manufacturing. So, **companies think M7/M8/M8.5 materials could be near-term sweet spots** for optical modules.

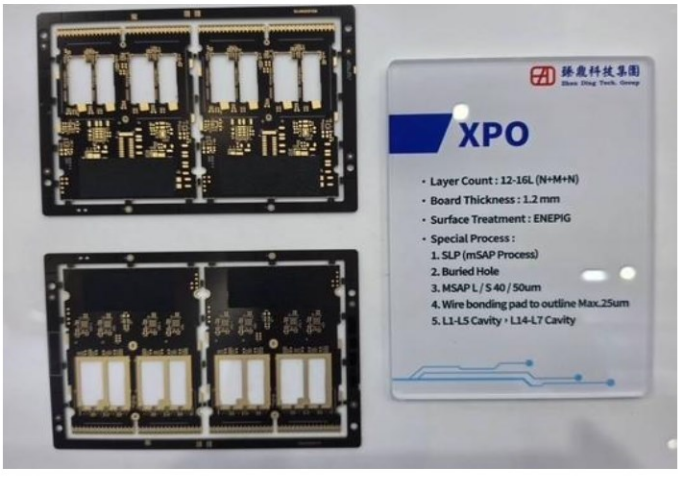
In 800G/1.6T optical module boards**, Doosan's market share is higher** than EMC's, but industry experts think **EMC's EM-536K** (M8+ level, with strong Df) could have potential to gain share in the generation of NPO or 3.2T.

Fig. 47: An illustration of optical package



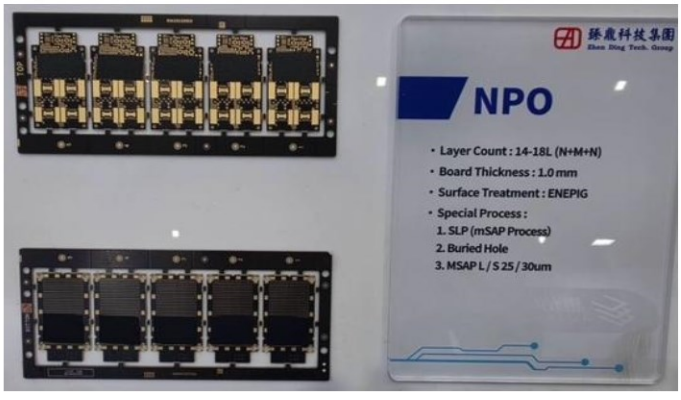
Source: ZDT, Nomura research

Fig. 48: ZDT XPO



Source: ZDT, Nomura research

Fig. 49: NPO



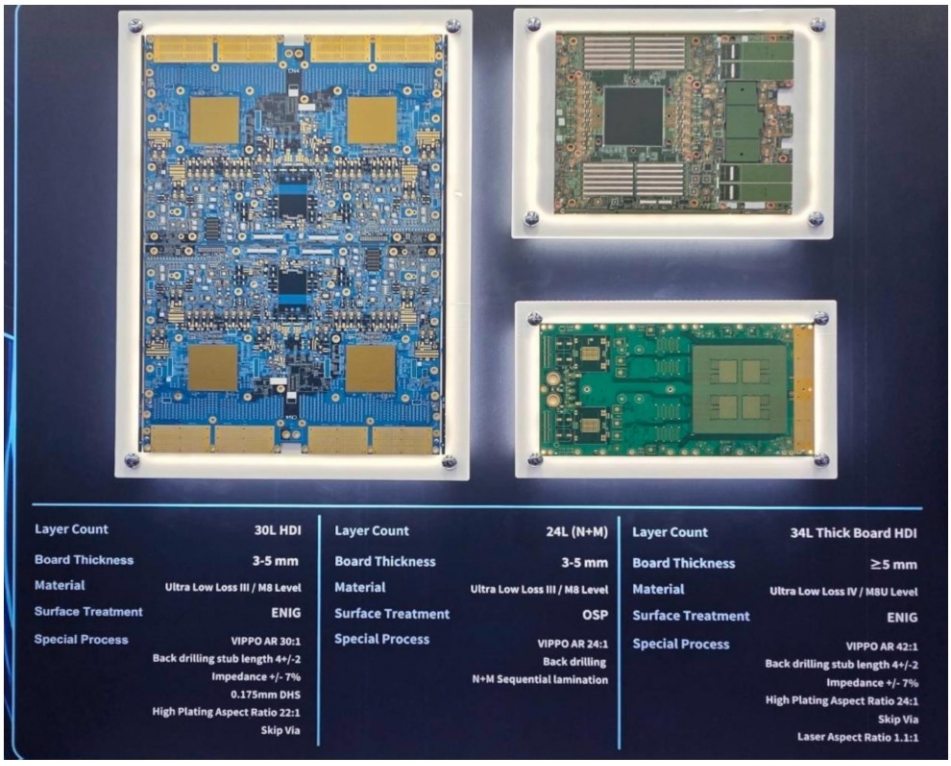
Source: ZDT, Nomura research

ZDT's HLC/HDI AI boards

ZDT demonstrated a 34L, HDI+3 or 4, AI ASIC compute board, with M8K2 hybrid materials and a thickness of >=5mm. Each board carries one GPU/ASIC with two NPO modules for scale-up connectivity. We believe this structure will be a typical design for one of the mainstream AI platforms.

ZDT also showed a 30L (HDI+1, M+N) switch board, with M8K2 materials. We believe that HDI mixed up with the M+N structure will become more popular in the future.

Fig. 50: ZDT HLC



Source: ZDT, Nomura research

Shortage

Likely ongoing lower-tier CCL price inflation due to material constraints

Considering all our observations above, we reason that electrical-grade glass (E-glass) supply constraints might persist throughout 2027F given insufficient loom availability at the fabric makers competing with Nittobo's T-glass expansion (whose allocation is likely prioritized by Toyota, as per our checks). YTD price hikes for M6 (and a portion of M7) and below CCL have been predicated on inflating E-glass quotes. As such, we could see further upside to lower-tier CCL pricing and GM profile into 2027F due to likely rising E-glass costs.

Admittedly, we believe the price discrepancy between E-glass and low-Dk 1 glass continues to shrink, and our feedback from the supply chain indicates that some fabric makers could thus mull over reallocating more capacity from low-Dk 1 to E-glass, possibly resulting in stagnant E-glass pricing at some point of time yet shortage in low Dk 1 glass (used in M7/M8 CCL). There might be a calibration of supply allocation to E-glass vs low-Dk 1 and consequent price dynamics change before the loom capacity is ultimately resolved, in our view.

Furthermore, we reason that low-end copper foil supply crunch might be another variable to drive lower-tier CCL pricing in 2027F as leading players in Japan and Taiwan are downsizing their standard product capacity to support HVLP.

High-end CCL makers should have more pricing power as well

While high-end CCL pricing schemes appear to be "more disciplined" even facing robust demand due to business reasons, we believe the major vendors are working toward at least one price renegotiation on a semi-annual basis. A major factor could be tighter HVLP4 supply given the ramp-up of AWS' Trainium 3, nVidia Vera Rubin, and AMD's (AMD US, Not rated) MI450. Our baseline assumption for EMC is another 10-20% price hike effective from 4Q26F.

What happens in case of unexpected demand surge?

All the imbalance scenarios above are implications based on what the supply chain already sees or expects to see. However, occasionally there could be unexpected demand streams incoming that exacerbate the already-wide supply gap – reminiscent of a sudden surge in general server CPU and networking switch in early 2026 which was unplanned in 2025. From our conversations with the supply chain last week, we are surprised that there might be some new AI/customized CPU platforms not yet identified by

PCB makers and their upstream material suppliers into 2027F, potentially sitting on decent volumes planned on the IC fabrication side. If the demand projection really prevails on to the board/system level, the industry shortage could end up becoming worse than our current assumptions.

Fig. 51: PCB, CCL and substrate supply chain matrix of major AI servers

		Google	AWS	Meta	Microsoft	nVidia	AMD
GPU/TPU/ ASIC substrate		Unimicron, Toppan, NYPCB, ZDT? EMIB-T: Ibiden, Unimicron, Shinko, AT&S?	Trainium: Unimicron, SEMCO Graviton: SEMCO, Toppan?	Unimicron, others?	Unimicron?	A100/H100: Ibiden Grace: Ibiden, Unimicron Blackwell: Ibiden, Unimicron Rubin: Ibiden, Unimicron, SEMCO	MI450/550: AT&S, Ibiden
AI GPU OAM	CCL	X	Panasonic, EMC? Tr3.5/5: EMC, NY?			Doosan	MI450/550: EMC, Doosan
	HDI		Shengyi, ZDT Tr3.5/4: GCE, ZDT, Shengyi?			Bianca: VGT, Unimicron, ZDT	MI450/550: SCC, Daeduck, Dynamic?
AI GPU UBB	CCL	Panasonic, EMC	EMC, TUC	EMC	EMC?	Doosan R200 HGX: EMC	EMC
	PCB	ISU, WUS, TTM, LCS, VGT, Unimicron, ZDT?	GCE, Shengyi, First Hi-tec	WUS, ISU, TTM	WUS, GCE, TTM?	WUS, TTM, ISU, VGT?	WUS, GCE?
General server (ASIC)	CCL	Panasonic, EMC, NY?			EMC		
	PCB	VGT, WUS, ISU, TTM, Tripod?			WUS, ISU, GCE?		
General server	CCL	Purley: ITEQ (170GRA1), TUC, Whitley: ITEQ (958G), EMC (EM526), others PCIe Gen 5: EMC (EM528), ITEQ (968G), others PCIe Gen 6: EMC (EM626), ITEQ (988GL), TUC (883A), others					
	PCB	GCE, WUS, TTM, ISU, ZDT, Tripod, Hannstar, and others					
Switch	CCL	400G: EM890k, Panasonic M7, Doosan, TUC T3 800G: EM892k, Panasonc M8, TUC T4				EMC, SYTECH, Doosan, Taiflex?	EMC, Doosan
	PCB	WUS, TTM, ISU, GCE, ZDT, and others				WUS, VGT, Unimicron, ZDT, TTM, Kinwong, others?	SCC, WUS, Daeduck

Source: Company data, Nomura estimates

Appendix A-1

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