October 30, 2026 01:49 PM GMT

Investor Presentation | Asia Pacific

Greater China Semiconductors: AI Semi Supply Chain, Memory, CPO, Quantum Security

Charlie Chan
Equity Analyst
Charlie.Chan@morganstanley.com +886 2 2730-1725

Daniel Yen, CFA
Equity Analyst
Daniel.Yen@morganstanley.com +886 2 2730-2863

Daisy Dai, CFA
Equity Analyst
Daisy.Dai@morganstanley.com +852 2848-7310

Lucas Wang
Equity Analyst
Lucas.Wang@morganstanley.com +886 2 2730-2875

Henry Zhao
Equity Analyst
Henry.Zhao@morganstanley.com +852 2239-7731

Ethan Jia
Research Associate
Ethan.Jia@morganstanley.com +852 3963-2287



the 2027 Extel Asia Research Survey. Voting opens 10 November 2026.

GREATER CHINA TECHNOLOGY SEMICONDUCTORS

Asia Pacific
Industry View **Attractive**

investors should be aware that the firm may have a conflict of

Research as only a single factor in making their investment decision.

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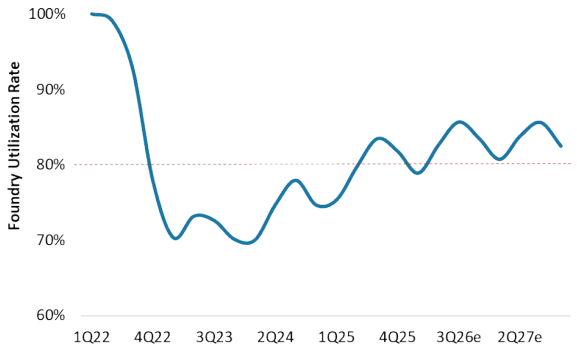
Strong AI Semi Outlook

Long-term demand drivers:

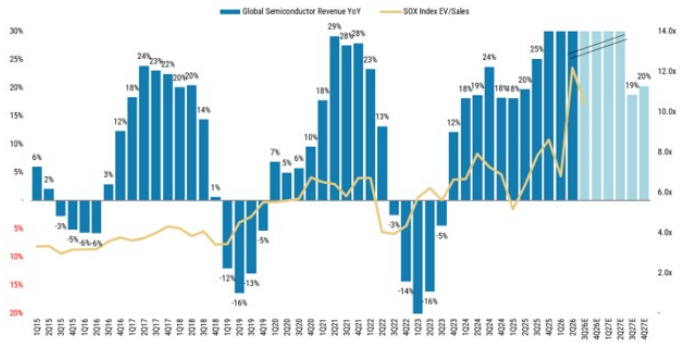
- **Chip inflation:** We expect “price elasticity” to affect demand for tech products. Rising wafer, OSAT and memory costs create more margin headwinds for chip designers in 2026.
- **AI cannibalization:** Besides demand weakness (AI replacing some human jobs), we see the semi supply chain also prioritizing AI semis over non-AI semis, e.g., T-Glass and memory shortages.
- **China – AI: DeepSeek is triggering inferencing AI demand:** DeepSeek has demonstrated cheaper inferencing. The local foundry supply chain is also becoming more capable in terms of AI GPU production.

Broader Semiconductor Cycle

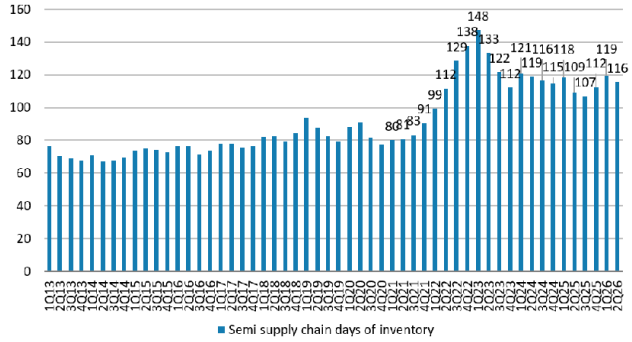
Logic semi foundry utilization could reach 80% in 2H26



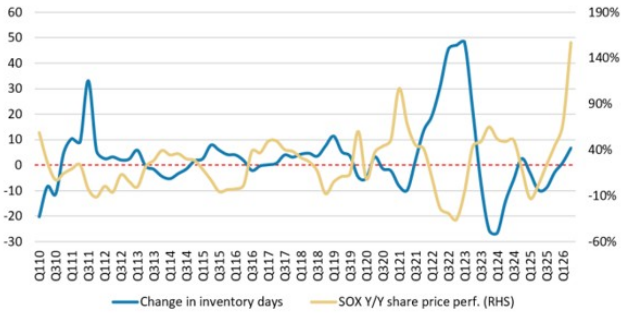
Excluding memory and NVIDIA's AI GPU revenue, non-AI semi growth is expected to decline in 2027



Semi supply chain – days of inventory as of 2Q26



Historically, when inventory days have gone down, the semi stock index has risen



TSMC 3Q26 Earnings Review

TSMC 3Q26 Earnings and 4Q26 Guidance Review

3Q26 earnings review

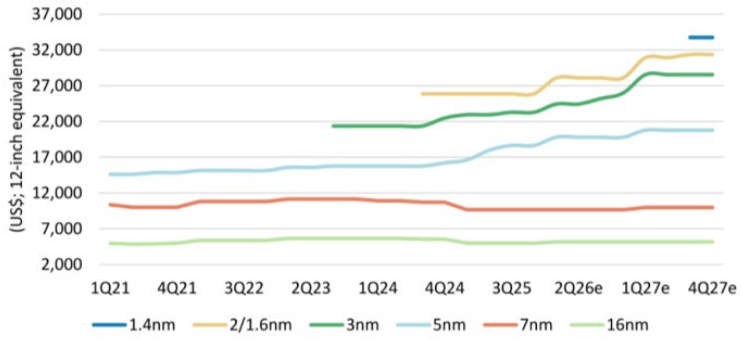
(NT$ mn)	3Q26				
	Actual	Q/Q	Y/Y	MS Est.	Consensus
Financials					
Revenue	1,494,243	17.6%	50.9%	1,499,073	1,461,784
Opex	(115,934)	23.7%	32.0%	(101,410)	(119,637)
EPS (NT$)	29.43	8.0%	68.7%	30.74	28.65
Ratios					
GM (%)	66.4%	-131bps	696bps	67.5%	66.5%
Opex (%)	7.8%	38bps	-112bps	6.8%	8.2%
OPM (%)	58.7%	-169bps	808bps	60.8%	58.4%

4Q26 guidance review

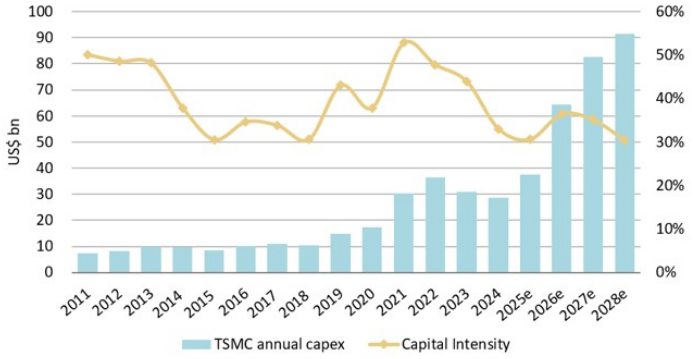
(NT$ mn)	4Q26				
	Guidance	MS Est.	Q/Q	Y/Y	Consensus
Financials					
Revenue	US$52.3bn to US$54.3bn, +14% Q/Q increase at mid-point	1,685,894	12.8%	61.2%	1,609,407
Opex		(107,433)	-7.3%	23.4%	(126,452)
EPS (NT$)		35.25	19.8%	80.8%	31.84
Ratios					
GM (%)	65.0% - 67.0%	68.6%	215bps	623bps	66.5%
Opex (%)		6.4%	-139bps	-195bps	7.9%
OPM (%)	56.5% - 58.5%	62.2%	353bps	819bps	58.7%

TSMC Could Hike Leading-edge Wafer Price by 5-10% in 2027 with Strong Capacity Expansion

TSMC wafer pricing trend

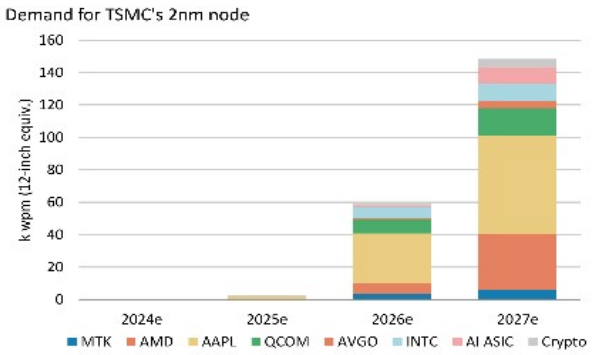


We raise 2027-28 capex forecasts to US$83bn and U$92bn, respectively

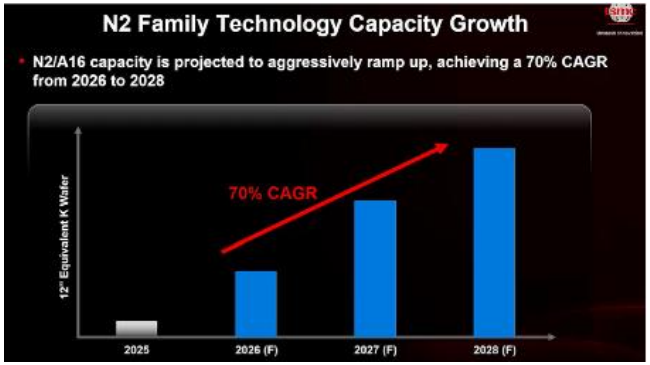


TSMC 2nm Demand Remains Strong

TSMC – Our projection of 2nm customer demand breakdown

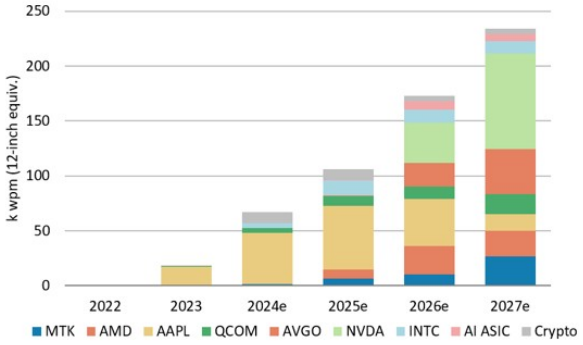


TSMC suggests N2 capacity to achieve 70% CAGR in 2026-2028e

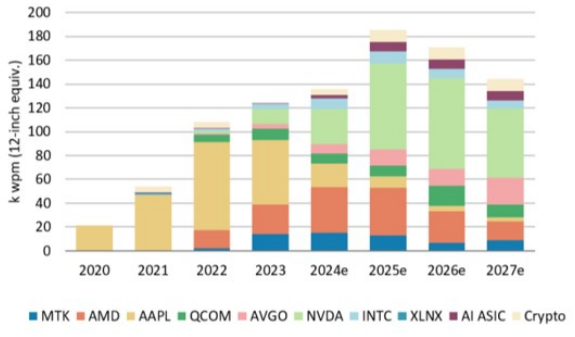


TSMC N5 Capacity to Drop in 2027 while N3 Should Keep Increasing, Similar to our Demand Forecast

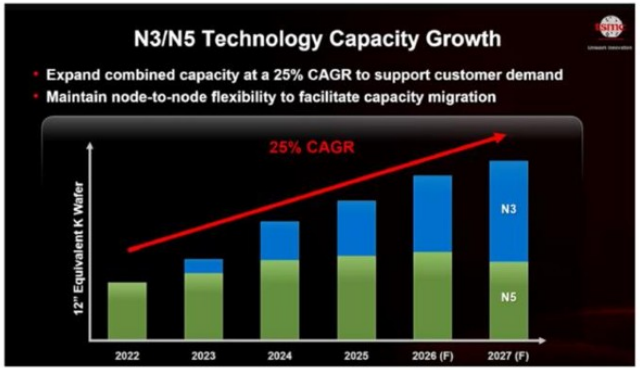
TSMC – MS projection of 3nm customer demand breakdown



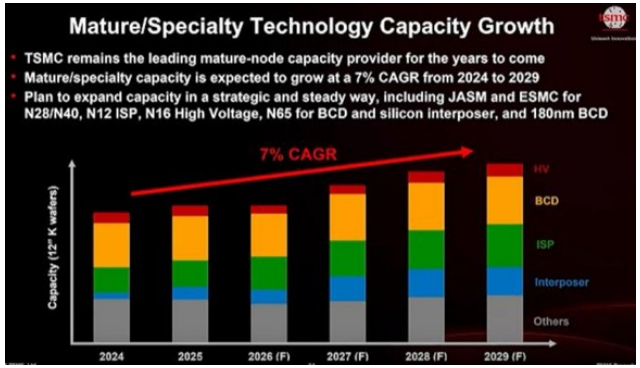
TSMC – MSprojection of 4/5nm customer demand breakdown



TSMC indicates that N5 capacity will drop in 2027 while N3 capacity should keep increasing

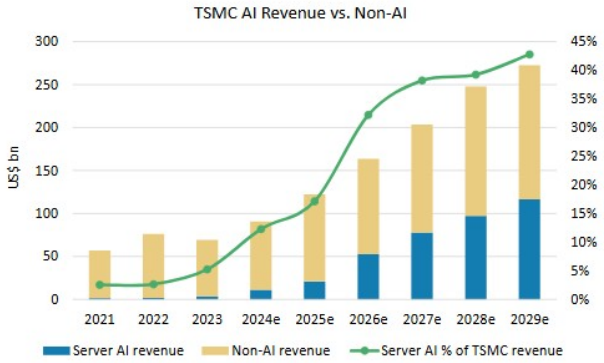


TSMC mature/specialty capacity CAGR 7% from 2024-29e

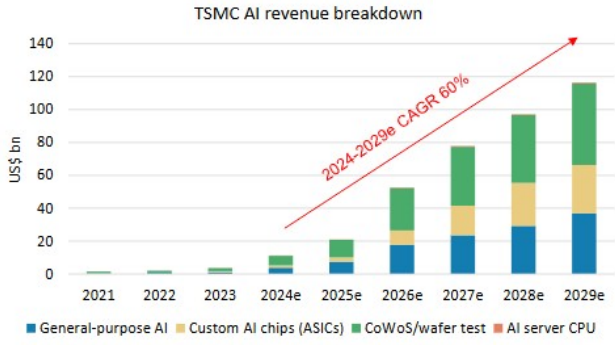


TSMC – AI Semis Revenue Could Reach 60% from 2024 to 2029e

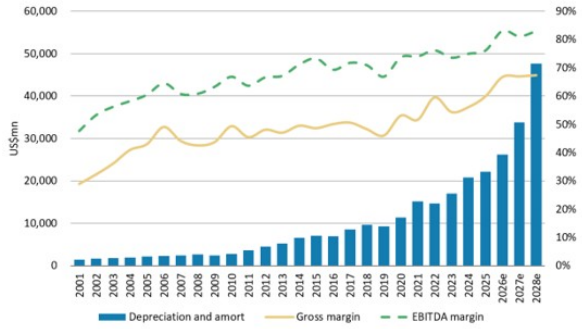
TSMC – AI semis revenue could account for >30% of 2026e revenue



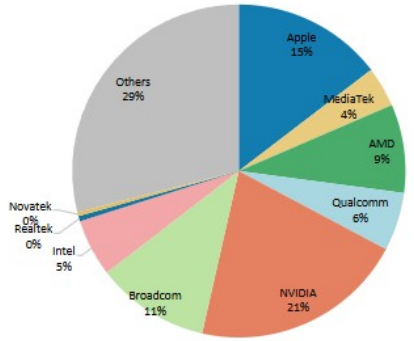
TSMC – AI semis revenue breakdown



TSMC – Margin expansion



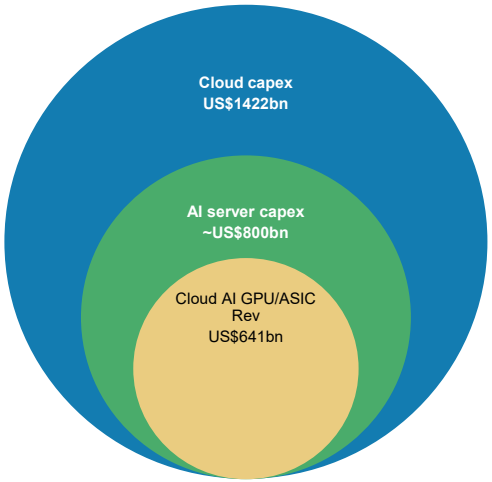
TSMC – 2026e revenue breakdown by customer



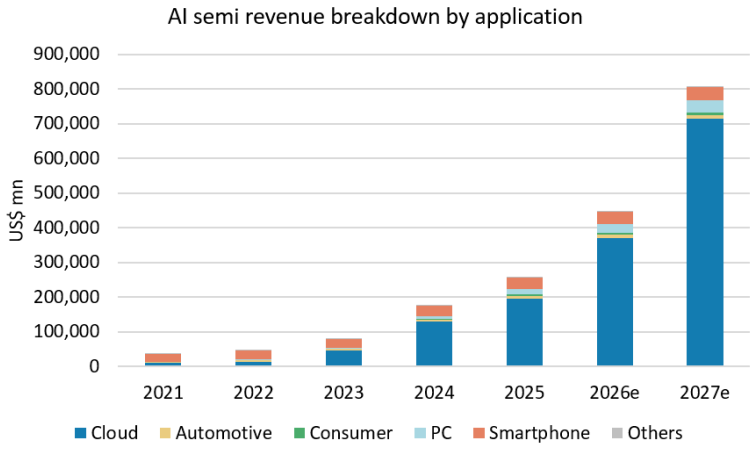
AI Semi Supply Chain and Niche Memory

Global Semi Industry Market Could Reach US$2.5tn in 2027e, with AI Semis Contributing 1/3

Our supply chain data-driven bull-case assumption is that cloud AI Semi TAM could grow to US$641bn in 2027e

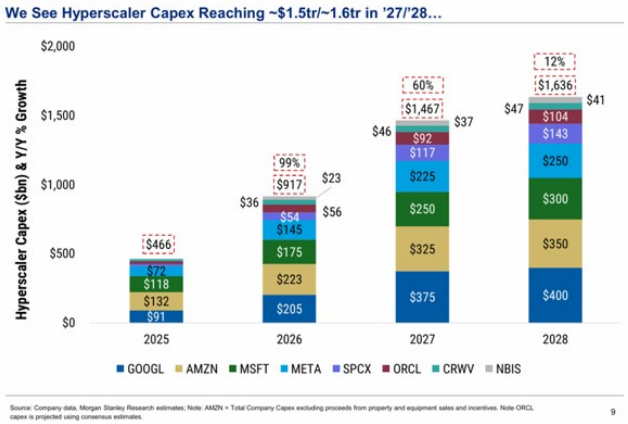


We expect AI semi TAM to reach ~US$809bn in 2027e

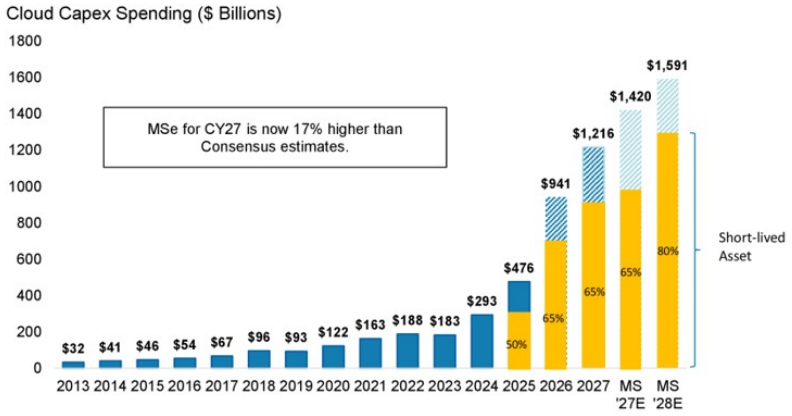


Deceleration of Cloud Capex From Major CSPs into 2028?

Hyperscaler capex breakdown by major CSP: In aggregate, total 12% growth seen for 2028



Morgan Stanley cloud capex tracker: We estimate nearly US$1.6tn of cloud capex in 2028 (top 14 listed global CSPs; no sovereign AI)



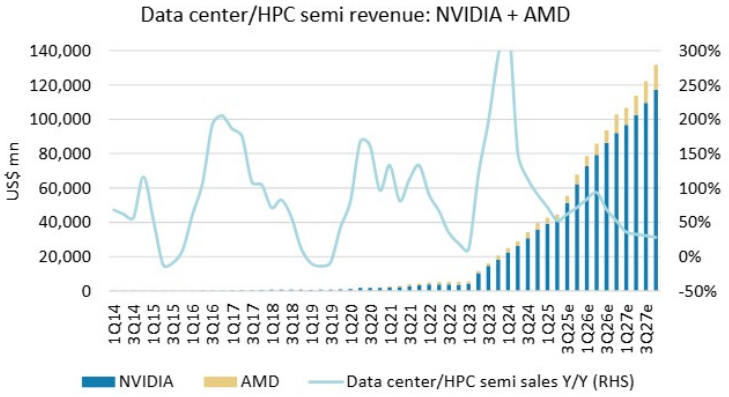
Source: FactSet, company data,

GPU Vendor P/E Multiple Might Catch up After Delivering Strong Revenue

P/E multiple trend of AI semis



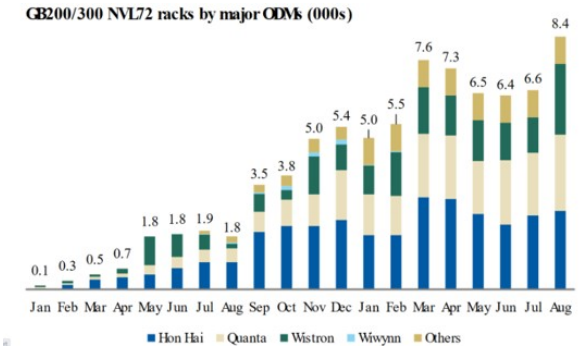
We still expect AI chip revenue to rise QoQ



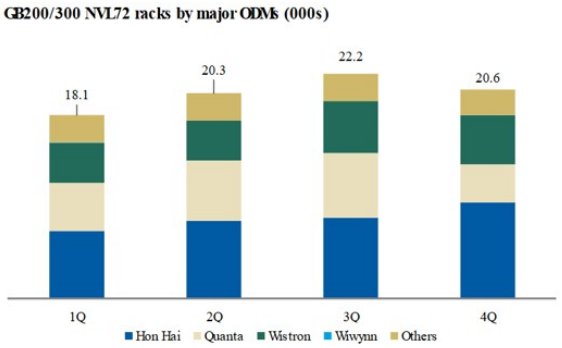
Source: FactSet, Company data,
Synopsys, Cadence, ASML, BESI, Ibiden, KYEC, Advantest.

NVIDIA NVL72 Rack Forecasts

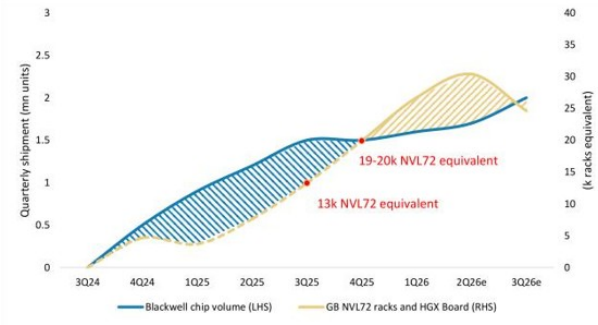
GB200/300 NVL72 Rack Ramp Monthly Trajectory

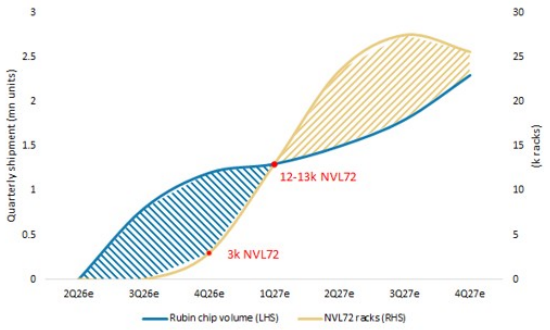


Industry-wide GB200/300 NVL72 Rack Split (2026)



We estimate that TSMC produced 5.1mn chips in 2025, with full-year GB200 NVL72 shipments seen reaching 30k

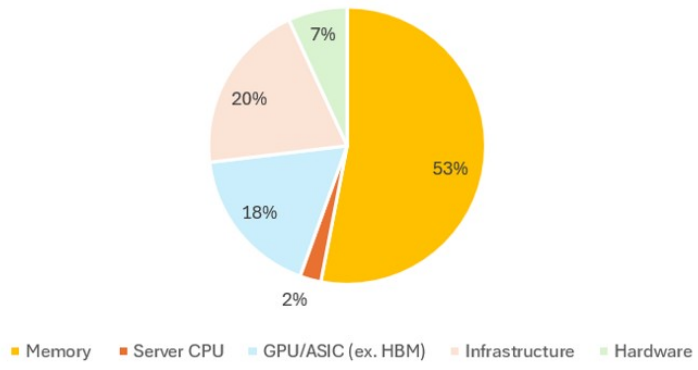




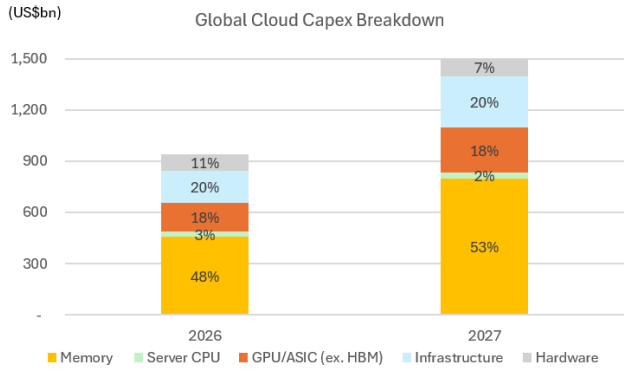
we include Wistron's computing tray (L10) rack equivalent number (without accounting for rack assembly and test times for L11). Estimates are from our Asia Pacific Tech team's downstream estimates.

Logic Cloud Accounts for Around 20% of Global Cloud Capex

2027 Cloud Capex Breakdown

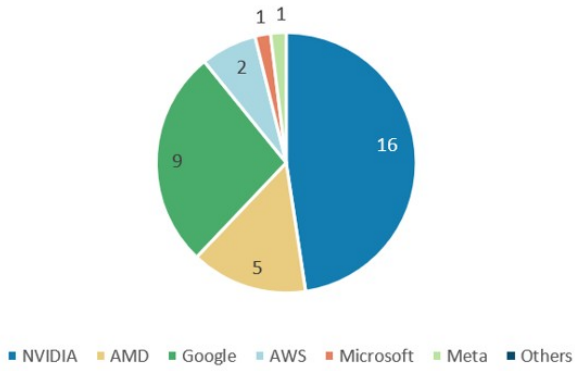


Global Cloud Capex Breakdown

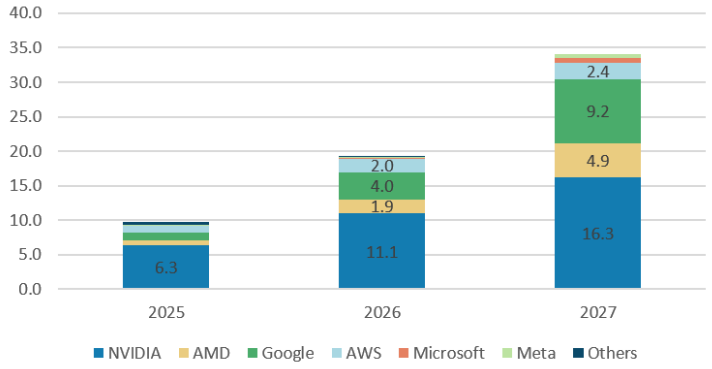


Power Consumption Growth Remains Robust

2027 GPU/ASIC total power consumption (GW)



Global GPU/ASIC Total Power Consumption from TSMC CoWoS Shipment



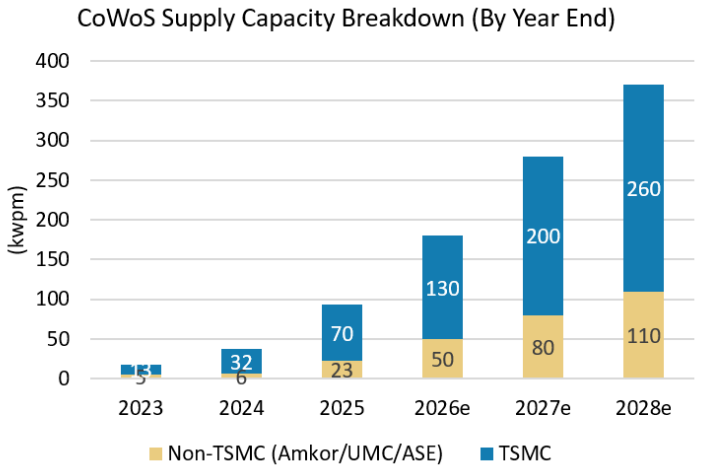
Announced Power Deployment – Implications for TSMC

Announced Power Deployment Implication for TSMC					
GPU/ASIC Vendor	NVIDIA (Top US AI firm)	AMD (Top US AI firm)	Broadcom	AWS (Top US AI firm)	NVIDIA (SpaceX)
Power Deployed (GW)	10	6	3.5	2	8
Rack name	Vera Rubin NVL144	Helios	TPU	Trainium3 UltraServers	Vera Rubin NVL144
Power consumption per Rack (kW)	220	220	63	144	220
Rack Number (k units)	45	27	56	14	36
Chip Name	Rubin GPU	MI455 GPU	TPUv7 (Ironwood) TPUv8i (Sunfish)	Trainium3 (4)	Rubin GPU
Chip Volume (k units)	3,273	1,964	3,571	2,000	2,618
Life Cycle for the project	3	3	5	8	1
Implied life-cycle CoWoS Volume (k wafers)	409	166	260	118	409
Implied life-cycle 2/3nm wafer Volume (k wafers)	260	95	190	107	208
2027 annual CoWoS demand (k wafers)	136	55	52	15	409

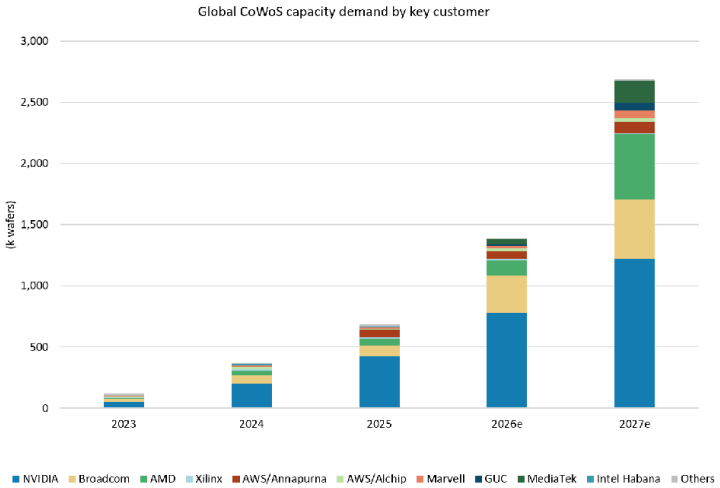
v8i per chip TDP being ~980W.

TSMC May Expand CoWoS Capacity to 260kwpm by 2028 Given Ongoing Strong AI Demand

Global CoWoS capacity expansion by year-end and by vendor



Global CoWoS consumption, by customer



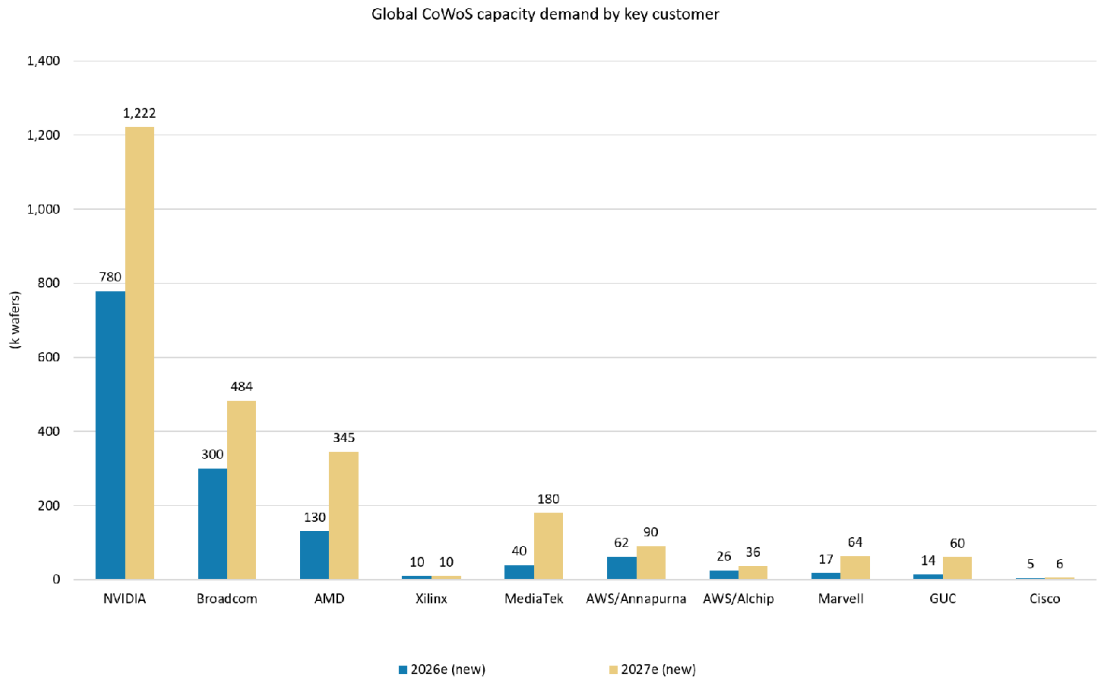
Global CoWoS Demand Breakdown

Factoring in NVIDIA chip price hike starting in 1Q27, 70%+ revenue growth in 2027 looks consistent with TSMC CoWoS implied chip shipments

(k wafer)	2023	2024	2025	2026e	2027e	2023	2024	2025e	2026e	2027e
NVIDIA	53	200	425	780	1,222	45%	54%	62%	56%	49%
TSMC			390	680	1,090					
CoWoS-L			390	650	910					
CoWoS-S			0	20	50					
CoWoS-R			0	10	130					
Non-TSMC			35	100	132					
Amkor			35	100	132					
CoWoS-S			20	20	12					
CoWoS-R			15	80	120					
ASE/SPIL			0	0	0					
CoWoS-S			0	0	0					
CoWoS-R			0	0	0					
Broadcom	23	68	85	300	484	20%	18%	12%	22%	19%
TSMC			83	260	420					
CoWoS-L			0	15	60					
CoWoS-S			83	245	360					
ASE/SPIL			2	30	40					
CoWoS-L			0	0	0					
CoWoS-S			2	30	40					
Amkor				10	24					
CoWoS-S				10	24					
AMD	7	40	60	130	345	6%	11%	9%	9%	14%
TSMC			60	80	215					
CoWoS-L			0	70	210					
CoWoS-S			60	10	5					
ASE/SPIL			0	50	110					
CoWoS-L			0	50	110					
Amkor				0	20					
CoWoS-L				0	20					

(k wafer)	2023	2024	2025	2026e	2027e	2023	2024	2025e	2026e	2027e
Xilinx	3	10	10	10	10	3%	3%	1%	1%	0%
MediaTek				40	180				3%	7%
TSMC				40	180					
CoWoS-S				40	180					
AWS/Annapurna			60	62	90				4%	4%
TSMC			60	32	54					
CoWoS-R			60	32	54					
ASE/SPIL				30	36					
CoWoS-R				30	36					
AWS/Alchip	9	16	5	26	36	8%	4%	1%	2%	1%
Intel Habana	0	7	9	0	0	0%	2%	1%	0%	0%
Marvell	1	18	15	17	64	1%	5%	2%	1%	3%
TSMC				5	50					
CoWoS-L				5	50					
CoWoS-R			15	0	0					
ASE/SPIL				12	14					
CoWoS-R				12	14					
GUC	1	1	2	14	60	1%	0%	0%	1%	2%
Cisco		2	3	5	6		1%	0%	0%	0%
Others	20	10	15	10	12	17%	3%	2%	1%	0%
Total demand	**117**	**372**	**689**	**1,394**	**2,509**	**100%**	**100%**	**100%**	**100%**	**100%**

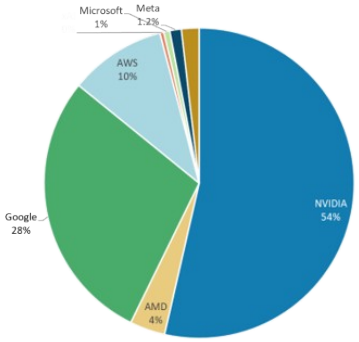
Global CoWoS Demand Set to Grow Robustly in 2027 at Each Major Customer



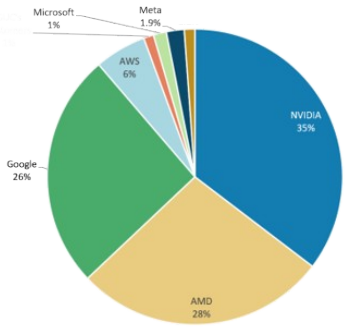
Source: Company

AI Computing Wafer Consumption Could Reach >US$55bn in 2027, with NVIDIA Accounting for the Majority

AI semi wafer consumption, by customer, 2026e



AI semi wafer consumption, by customer, 2027e

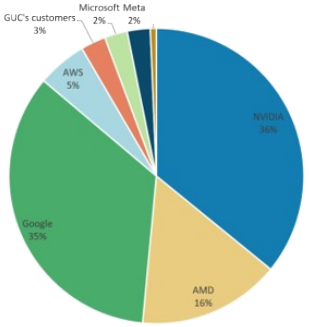


AI chip vendor	Product name	CoWoS capacity allocation (k wafers)	Chips per CoWoS wafer	Implied shipments (k)	Compute die size	Geometry	Compute die units	Wafer consumption (k wafers)	Wafer price (US$)	Wafer revenue TAM (US$ mn)
AI GPU (2027e)										
NVIDIA	B300	40	14	560	850	4nm	2	44	23,042	1,024
	Vera CPU	250	23	5,750	850	3nm	1	228	27,300	6,229
	Rubin R200	740	8	5,920	850	3nm	2	470	27,300	12,827
	Rubin Ultra	130	8	1,040	850	3nm	2	83	27,300	2,253
AMD	MI350 series	5	12	60	110	3nm	8	2	27,300	48
	MI455	75	7	525	850	2nm	2	56	30,000	1,667
	MI450 (for Meta)	45	14	630	850	2nm	1	33	30,000	1,000
	MI500 (Arcadia)	10	4	40	850	2nm	2	4	30,000	127
	Venice CPU	210	21	4,410	155	2nm	8	176	30,000	5,292
AI ASIC (2027e)										
Google	TPU v7p (Ironwood; AVGO)	13	16	208	700	3nm	2	14	27,300	371
	TPU v8i (Sunfish; AVGO)	330	12	3,960	800	3nm	2	296	27,300	8,075
	TPU v8t (Zebrafish; MediaTek)	180	20	3,600	800	3nm	2	269	27,300	7,341
	TPU v9 (Humufish; MediaTek)			400	850	2nm	4	63	30,000	1,905
AWS	Trainium 3	140	17	2,380	700	3nm	2	127	27,300	3,465
Microsoft	Maia 200	5	29	145	700	3nm	1	3.8	27,300	103
	Maia 300	50	11	550	850	2nm	1	29.1	30,000	873
Meta	MTIA 3 (Iris)	55	10	550	850	3nm	2	44	27,300	1,192
US AI Lab	Nexus (Titan 1)	25	13	325	750	3nm	4	45.5	26,000	1,183
	Titan 2	5	8	40	850	2nm	4	8.5	30,000	254
Others		18								
Total		**2,454**						**1,996**		**55,230**

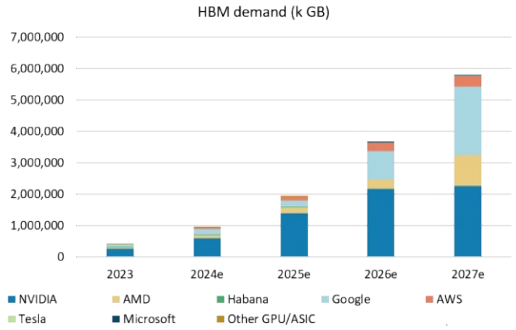
Source: Company

HBM Consumption in 2027e – Up to 44bn Gb

HBM consumption by customer in 2027e



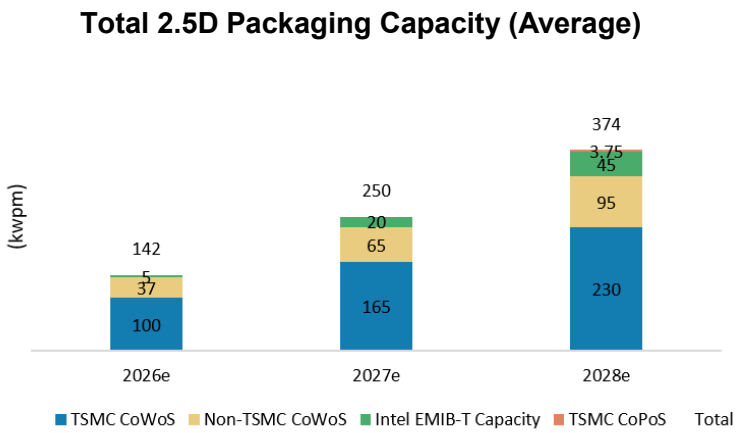
NVIDIA still consumes most HBM supply in 2027e

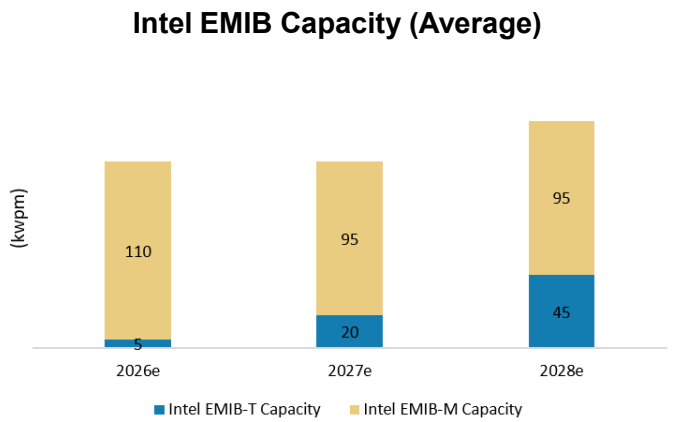


AI chip vendor	Product name	CoWoS capacity allocation (k wafers)	Chips per CoWoS wafer	Implied shipments (k)	HBM chip density (GB)	HBM chip units	Total HBM size (GB)	HBM generation	HBM vendor	Total HBM demand (k GB)
AI GPU (2027e)										
NVIDIA	B300	40	14	560	36	8	288	HBM3e 12hi	Hynix/Micron	161,280
	Vera CPU	250	23	5,750						
	Rubin R200	740	8	5,920	36	8	288	HBM4 12hi	Hynix/Micron/Samsung	1,704,960
	Rubin Ultra	130	8	1,040	48	8	384	HBM4e 12hi	Hynix/Micron/Samsung	399,360
AMD	MI350 series	5	12	60	36	8	288	HBM3e 12hi	Samsung/Micron	17,280
	MI455	75	7	525	36	12	432	HBM4 12hi	Samsung/Micron	226,800
	MI450 (for Meta)	45	14	630	36	6	216	HBM4 12hi	Samsung/Micron	136,080
	MI500 (Arcadia)	10	4	40	48	16	768	HBM4e 12hi	Samsung/Micron	30,720
	Venice CPU	210	21	4,410						
AI ASIC (2027e)										
Google	TPU v7p (Ironwood; AVGO)	13	16	208	24	8	192	HBM3e 8hi	Hynix/Samsung	39,936
	TPU v8i (Sunfish; AVGO)	330	12	3,960	36	8	288	HBM3e 12hi	Samsung/Hynix/Micron	1,140,480
	TPU v8t (Zebrafish; MediaTek)	180	20	3,600	36	6	216	HBM3e 12hi	Samsung/Hynix/Micron	777,600
	TPU v9 (Humufish; MediaTek)			400	48	12	576	HBM4e 12hi	Samsung/Hynix/Micron	230,400
AWS	Trainium 3	140	17	2,380	36	4	144	HBM3e 12hi	Hynix/Samsung/Micron	342,720
Microsoft	Maia 200	5	29	145	16	4	64	HBM3	Samsung	9,280
	Maia 300	50	11	550	36	8	288	HBM4 12hi	Samsung	158,400
Meta	MTIA 3 (Iris)	55	10	550	36	8	288	HBM3e 12hi	Samsung/Hynix/Micron	158,400
US AI Lab	Nexus (Titan 1)	25	13	325	36	6	216	HBM4 12hi	Samsung/Hynix/Micron	70,200
	Titan 2	5	8	40	36	8	288	HBM4 12hi	Samsung/Hynix/Micron	11,520
Others		18								
Total		**2,454**								**5,615,416**
									Total HBM demand (mn Gb)	**44,923**



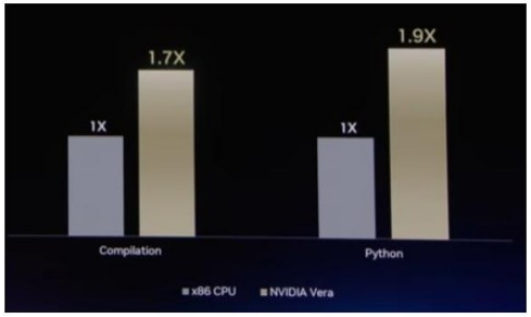
Total 2.5D Packaging Capacity Could Still Reach 50% YoY Growth in 2028



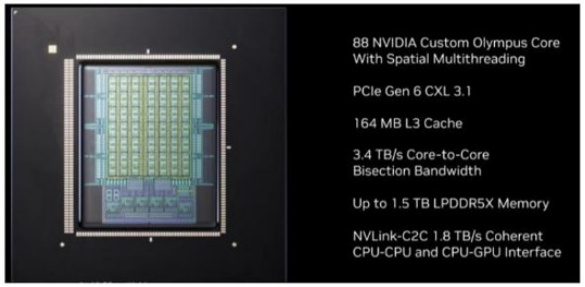


NVIDIA's Latest Vera CPU Could Support Robust Agentic CPU Demand

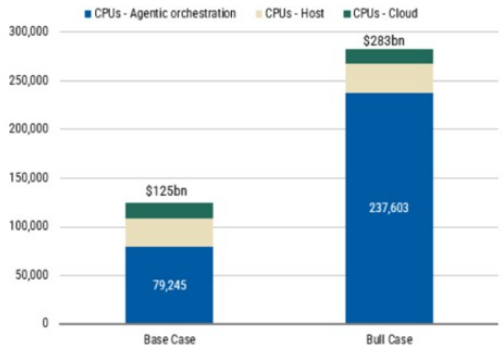
Vera performance could be 1.8x that of highest-performance x86 CPU



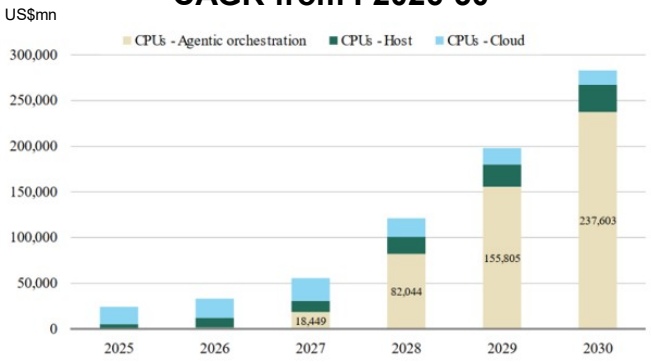
Vera CPU cores are not split across chiplets, enabling faster core-to-core connection



Our bull case implies a US$238bn CPU orchestration TAM



In MS top-down model, we estimate the Agentic CPU TAM will expand at a 251% CAGR from F2026-30



Global Technology: Agentic AI – The Surge Begins (11 May 2026)

AI ASIC and Chip Testing

AI Semis: Now and the Future – "Prompts"

- Generative AI Demand Driver:
    - Killer apps
    - Competition
    - Sovereign
- Growth limitations:
    1. Budget
    2. Energy -> in the US
    3. Chip Capacity -> in China
    4. Regulation
- Semiconductor solutions:
    - Moore's Law
    - CoWoS/ SoIC
    - HBM
    - CPO
    - Custom chip
    - GaN HVDC 800V
- Growth perspective:
    1. Inference vs. Training AI semis
    2. Edge vs. Cloud AI semis
    3. Custom ASIC vs. AI GPU

CSPs Still Need Custom Chips, Even with NVIDIA Providing Powerful AI GPUs

Global CSP cloud AI custom chips

Google TPU entering 6th generation



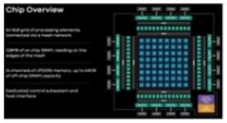
AWS AI training solution Trainium



AWS AI training solution Inferentia



Meta MTIA v1 with RISC-V cores



Habana developed the Gaudi chip



Tesla is introducing Dojos



The volume upside of AI chips like Google TPU could depend on ABF substrate supply



Alchip Might Achieve US$8bn Revenue for Trainium4 in 2028

Alchip 2028 Trainium revenue could reach US$8bn

		2026e	2027e	2028e
Volume (k)	Trainium3	400	600	
	Trainium4			800
Chip ASP Recognized by Alchip (US$k)	Trainium3	4.6	4.6	
	Trainium4			10
Trainium Revenue (US$bn)	Trainium3	1.8	2.8	
	Trainium4			8
	Total Trainium Revenue	1.8	2.8	8
Total Alchip Revenue (US$bn)		3.1	4.4	9.8
Trainium Revenue %		60%	63%	82%

Trainium forecasts from our Asian Research team

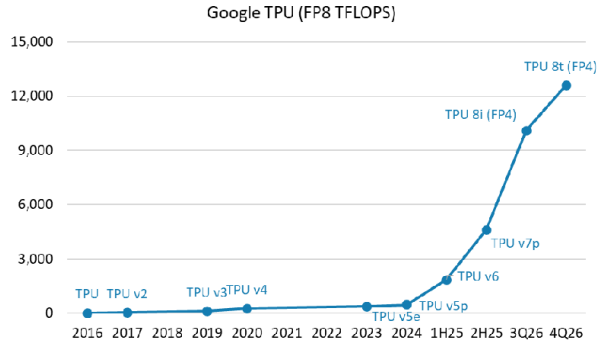
k Units	2023	2024	2025e	2026e	2027e	2028e
Trainium1/Inferentia2	300	600	30			
Trainium2		300	1,200			
Trainium3			85	1,700	2,380	-
Trainium4					unknown	2,500
Total	**300**	**900**	**1,315**	**1,700**	**2,380**	**2,500**

More ASIC Projects Are Coming, According to Each CSP Plan

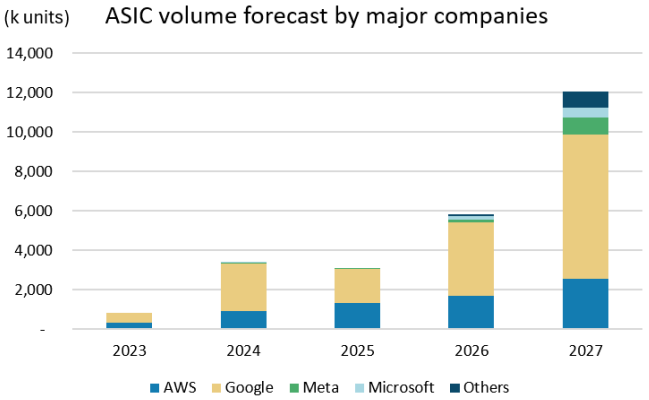
TPU Forecasts from MS Asia Research team

k Units	2023	2024	2025e	2026e	2027e	2028e
v5	500	2,400	250			
v6 (Trillium)			1,200			
v8t (Zebrafish; 3nm, by MediaTek)				500	3,000	2,000
v9 (Humufish; 2nm EMIB-T, by MediaTek)						3,000
v10 (Icefish; 1.4nm, by MediaTek)						unknown
Total	**500**	**2,400**	**1,750**	**3,300**	**7,500**	**>9000**

Google's TPU performance is growing rapidly

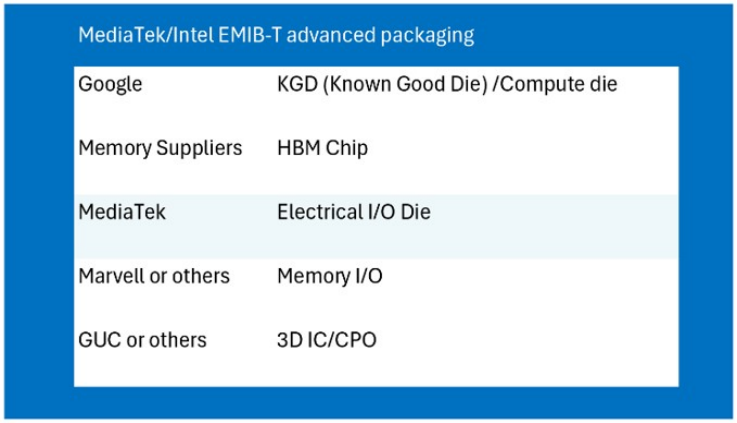


ASIC volume forecast by major companies



MediaTek TPU Revenue Could Reach US$70bn by 2029 Even Under a COT Model

We believe MediaTek would still at least handle the packaging and I/O die for TPU v10



We expect MediaTek 2029 TPU revenue to reach US$70bn

		2027e	2028e	2029e
Volume (mn)	TPU v8t (Zebrafish)	3	2	
	TPU v9 (Humufish; EMIB-T)		3	4
	TPU v10 (Icefish)			1
	2nd Customer Subsystem		0.1	0.5
Chip ASP Recognized by MediaTek (US$k)	TPU v8t	4.5	4.5	
	TPU v9; EMIB-T		13	13
	TPU v10			18
	2nd Customer Subsystem		25	25
Revenue (US$bn)	TPU v8t	13.5	9	
	TPU v9; EMIB-T		39	52
	TPU v10			18
	Total TPU Revenue	13.5	48	70
	2nd Customer Subsystem		2.5	12.5
Total MediaTek Revenue (US$bn)		35	75	NA
AI ASIC Revenue %		38%	68%	NA

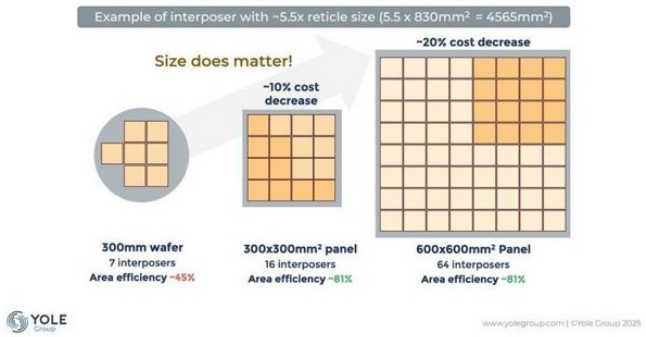
KYEC Benefits from Strong AI GPU, TPU and CPU Growth

AI Revenue Forecast for KYEC

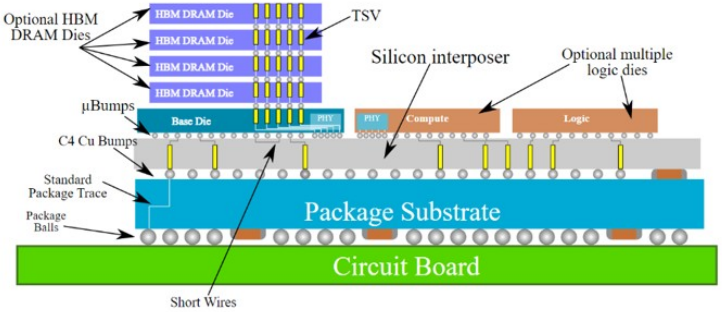
	1Q25	2Q25	3Q25	4Q25	1Q26	2Q26e	3Q26e	4Q26e		2025	2026e	2027e
Units (k)												
H-series	650	200	250	500	400	400	600	600		1,600	2,000	
B-series with GDDR7	-	-	300	500	250	250	250	250		800	1,000	
B-series with HBM	1,000	1,100	1,400	1,500	1,500	1,500	1,600	300		5,000	4,900	560
R-series							800	1,200			2,000	6,500
G-series CPU										1,100	2,450	250
V-series CPU											2,500	5,750
Google TPU										1,750	3,680	4,500
Google CPU											1,200	4,000
Test time												
Per chip test time (seconds)												
H-series test time	350	350	350	350	350	350	350	350		350	350	350
B-series with GDDR7 test time			350	350	350	350	350	350		350	350	350
B-series with HBM test time	700	750	900	1,000	1,000	1,000	850	850		1,000	850	850
R-series test time							850	850			850	1,275
G-series CPU test time										300	300	300
V-series CPU test time											700	700
Google TPU blended test time										186	340	450
Google CPU test time											300	400
Total test demand (k hrs)												
H-series	63	19	24	49	39	39	58	58		156	194	-
B-series with GDDR7			29	49	24	24	24	24		78	97	-
B-series with HBM	194	229	350	417	417	417	378	71		1,190	1,282	132
R-series					-	-	189	283			472	2,302
G-series CPU										92	204	21
V-series CPU											486	1,118
Google TPU										90	348	563
Google CPU											100	444
Test hour rate (for the largest customer including burn-in)	***170***	***170***	***170***	***170***	***170***	***170***	***180***	***190***		***170***	***178***	***200***
Test hour rate (for TPU with self-bought testers)										***200***	***250***	***280***
Largest customer's AI revenue to KYEC (US$ mn)	43.8	42.3	68.6	87.4	81.6	81.6	116.9	83.0		257.6	485.5	714.6
% of KYEC MSe Revenue (quarterly figures without CPU)	19%	15%	23%	27%	25%	23%	30%	18%		23%	32%	33%
TPU revenue to KYEC (US$ mn)										18.1	86.9	157.5
% of KYEC MSe Revenue										1.6%	5.7%	7.3%
Google CPU revenue to KYEC (US$ mn)											25.0	124.4
% of KYEC MSe Revenue											1.6%	5.7%

What About the Competition Between TSMC's CoWoS and Intel's EMIB?

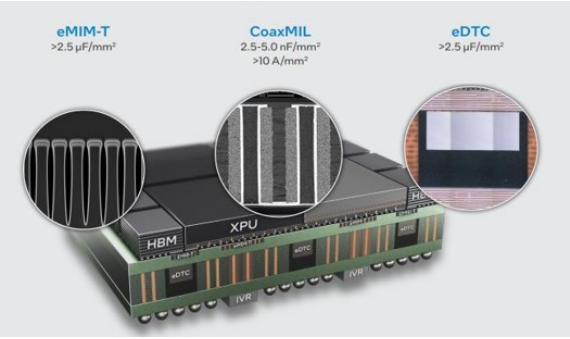
TSMC CoWoS can support up to 9.5x reticles, or four chips per wafer



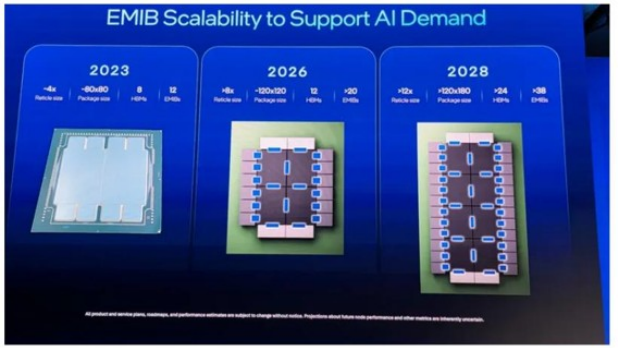
TSMC's CoWoS-S (silicon interposer) packaging architecture



Intel EMIB eDTC: APMemory's technology

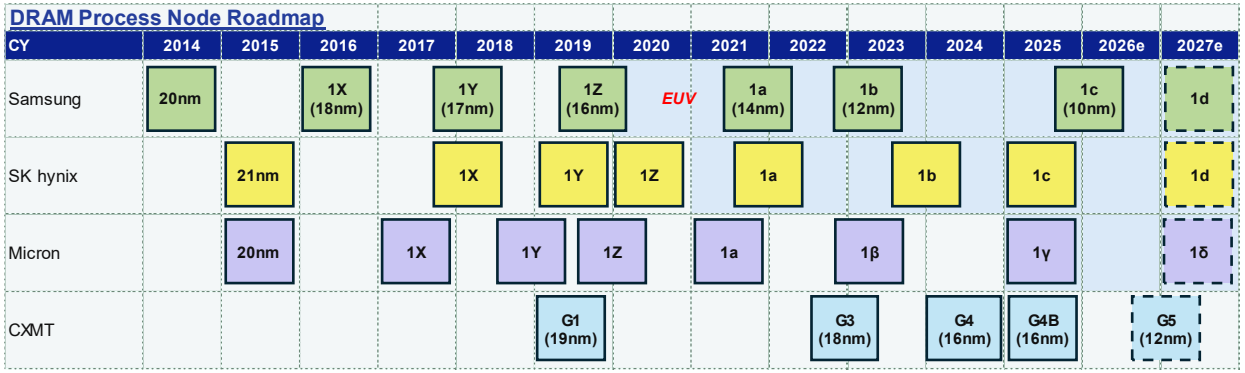


Intel's EMIB can support larger chips with more reticles (>12) if its supply chain can execute well



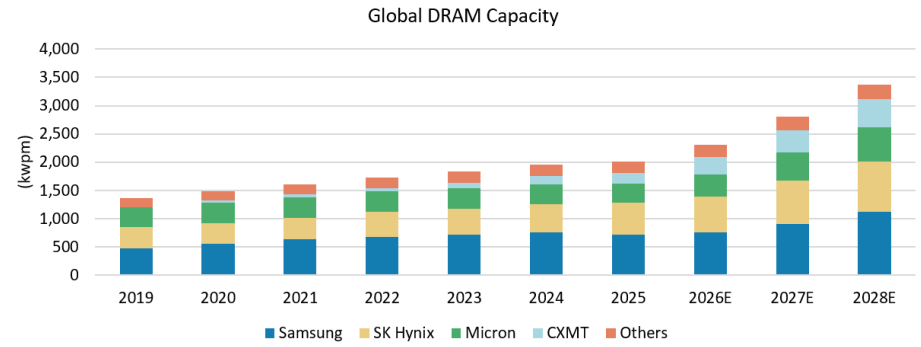
CXMT in the Context of Global DRAM

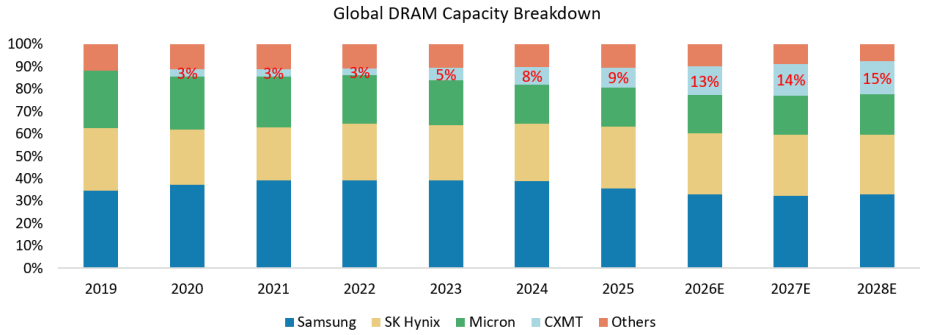
CXMT's Process Node Roadmap and Specs Compared to Global Vendors



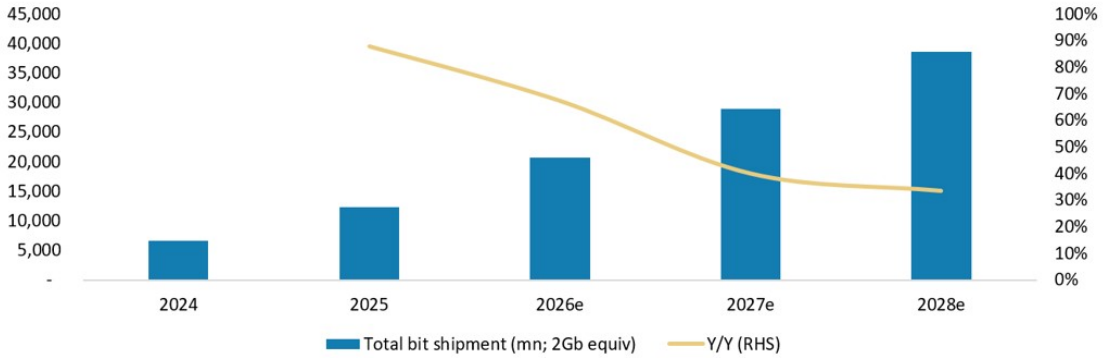
DDR5 Spec Comparison				
Manufacturer 16 Gb DDR5	Samsung 16 Gb DDR5	SK hynix 16 Gb DDR5	Micron 16 Gb DDR5	CXMT 16 Gb DDR5
Year First Revealed (Clock Speed, ex.)	2021DDR5-5600, DDR5-6000	2021DDR5-4800, DDR5-6000	2021DDR5-4800	2024DDR5-6000
Parent Product Examples	G.SKILL Trident Z5 DDR5 F5-5600U3636C16GX2-TZ5K (K4RAH086VB-BCQK)	SK Hynix 32 GB HMCG88MEBUA81N DDR5 UDIMM PC5-4800B module (H5CG48MEBD-X014)	TeamGroup ELITE DDR516 GB UDIMM (MT60B2G8HB-48B:A)	Gloway 16GB×2 (32GB) DDR5-6000 Module(H2G08SC522-6AF)
DRAM Process / Geometry	D1y (17nm)	D1y (17nm)	D1z (16nm)	G4 (16nm)
Die Size (Scaled)	73.58 mm² (8.94 mm × 8.23 mm)	75.21 mm² (9.24 mm × 8.14 mm)	66.26 mm² (8.43 mm × 7.86 mm)	66.99 mm² (8.19 mm × 8.18 mm)
Bit Density	0.217 Gb/mm²	0.213 Gb/mm²	0.241 Gb/mm²	0.239 Gb/mm²
Peripheral Gate Process	HKMG (Gate-first)	Poly/W Gate	Poly/W Gate	Poly/W Gate

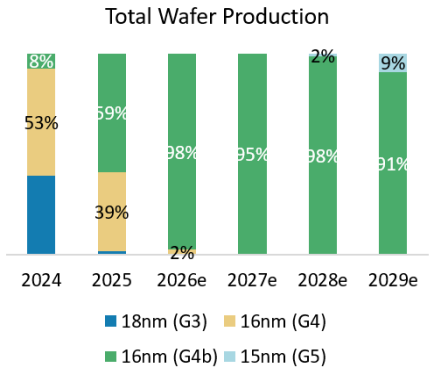
Global DRAM Capacity to Reach 3,374kwpm in 2028e, while CXMT May Account for 15% of That (Around 500kwpm by 2028)

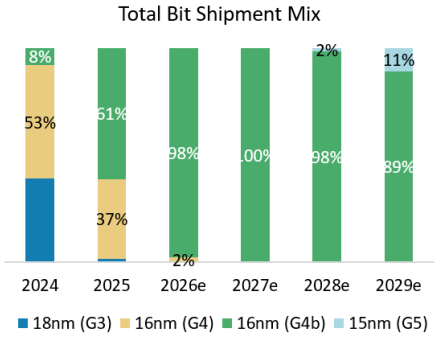




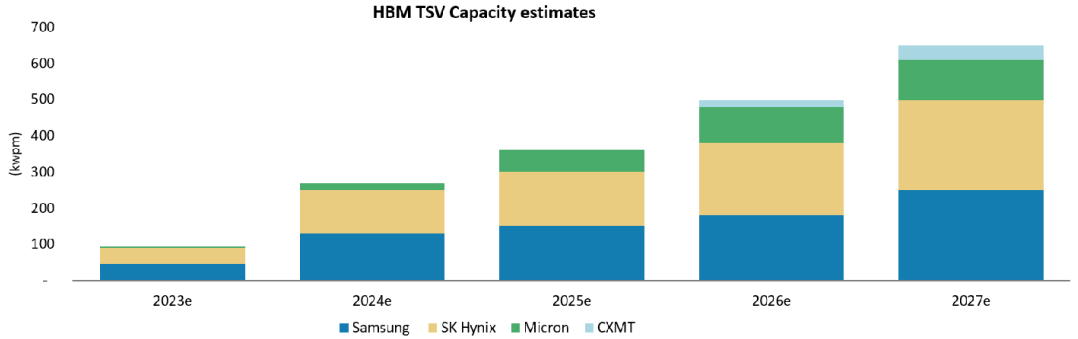
CXMT's Total Bit Shipments to Rise at a 40% CAGR in 2025-28e, as Production Mix Shifts from G4b to G5 into 2028-29

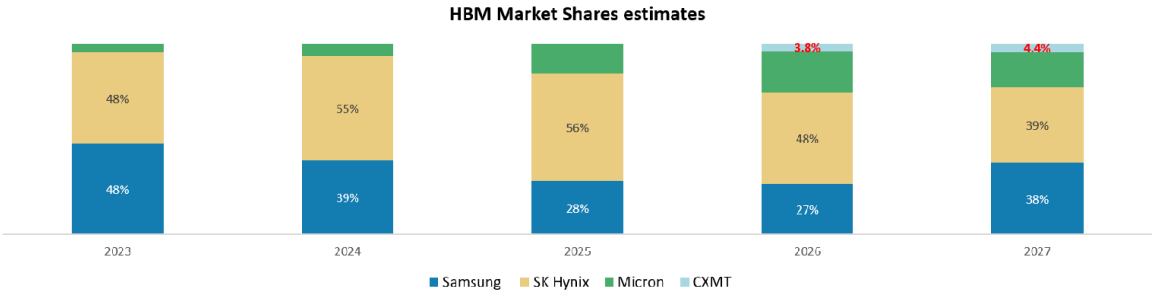






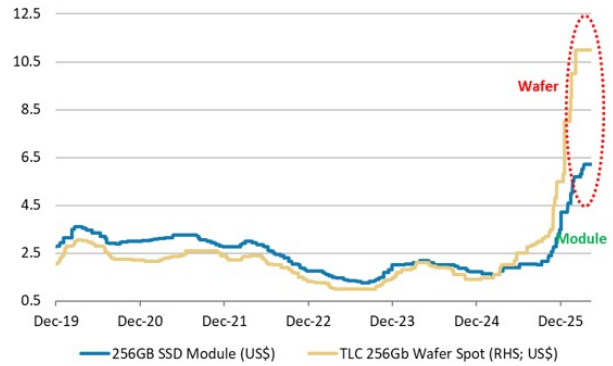
CXMT's HBM TSV Capacity to Reach 20kwpm in 2026e, 40kwpm in 2027e and 70kwpm in 2028e; to Account for 3.8% in 2026e and 4.4% 2027e of the Total HBM Market in Terms of Bit Shipment



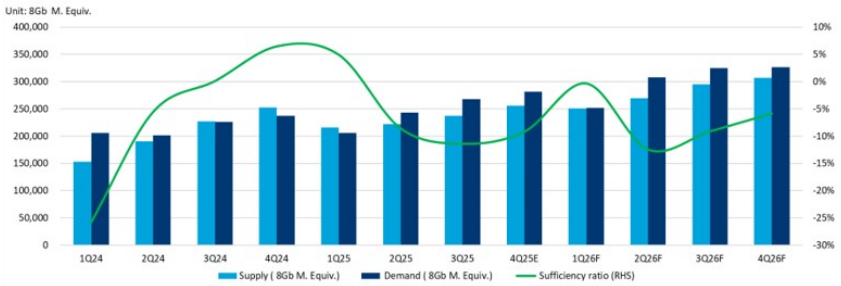


AI Storage Leads to NAND Shortage; We Also Expect NOR Flash Undersupply into 2026

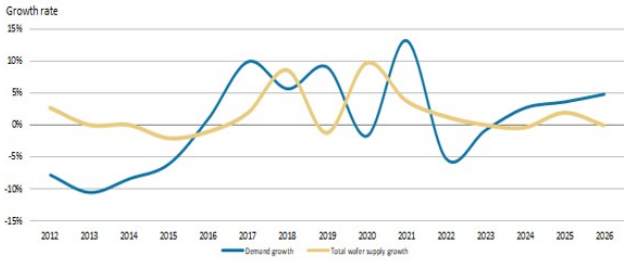
NAND wafer spot pricing and module prices



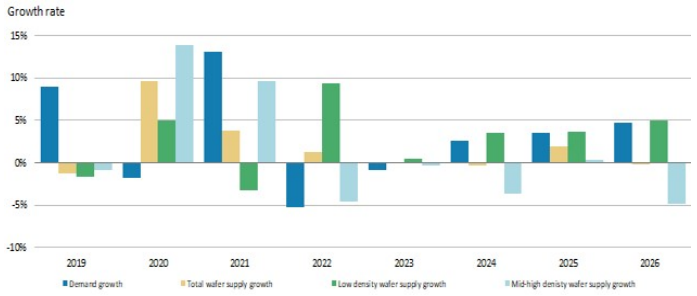
NAND supply and demand model



NOR flash demand and supply growth rates

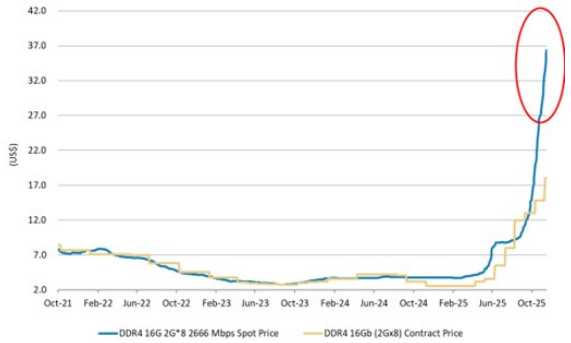


NOR flash demand and supply growth rates

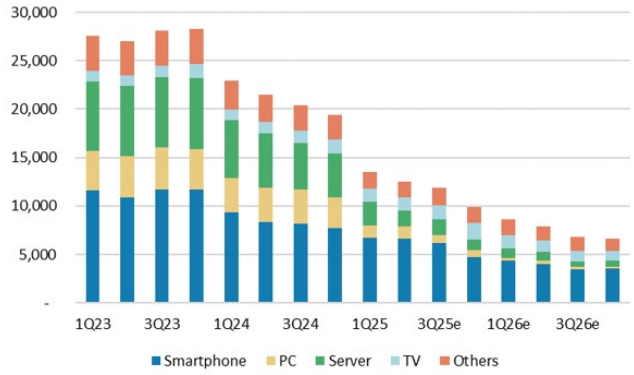


DDR4 Shortage to Persist into 2H26; Spot Price Capped

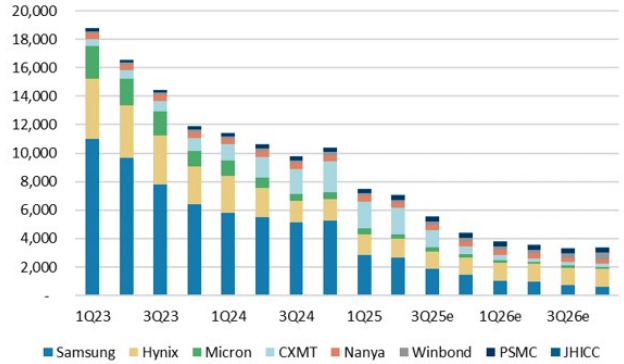
DDR4 16Gb spot vs. contract price



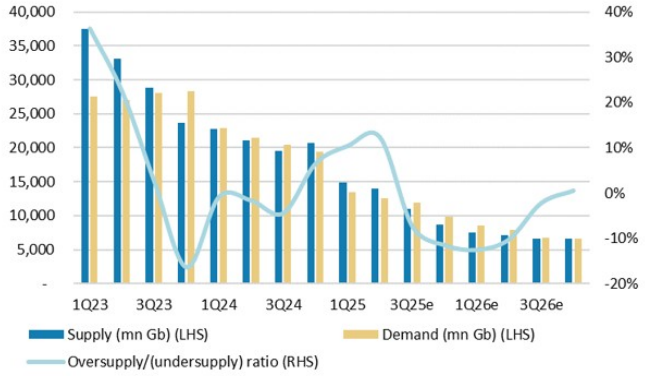
Quarterly demand breakdown, by product (mn Gb)



Quarterly supply breakdown (mn Gb)



Quarterly supply and demand summary



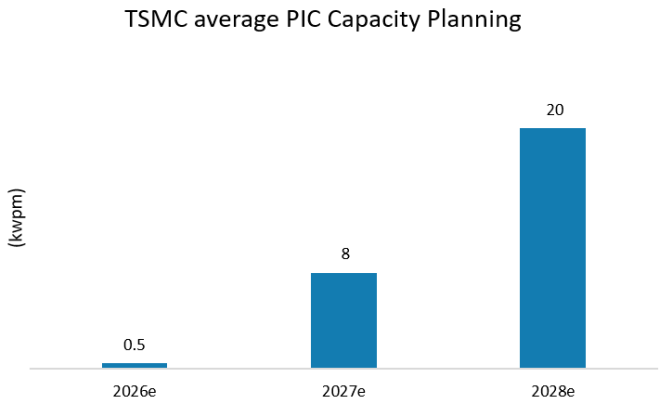
CPO

Larger OE TAM but Potentially Less Market Share for FOCI

Available OE estimates

	2026e	2027e	2028e
TSMC average PIC capacity (kwpm)	0.5	8	20
Die per wafer	648	648	648
Annual PIC production (mn)	4	62	156
SoIC yield rate	50%	95%	95%
Optical engine production (mn)	2	59	148
Downstream assembly yield rate	20%	30%	50%
Actual Optical engine shipment (mn)	0.39	17.73	73.87

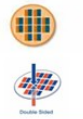
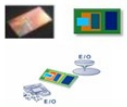
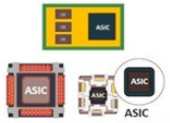
TSMC average PIC capacity



NVIDIA revenue contribution to FOCI

	2026e	2027e	2028e
Rubin Ultra rack unit (k units)		5	20
Optical Engine content per Rubin Ultra rack		3072	3072
Scale-Up (NVLink switch/Quantum)		2304	2304
Scale-out (Spectrum)		768	768
Other scale-out switch optical engine consumption			
Spectrum-X (k units)	800	1,000	3,000
Quantum-X (k units)		1,000	3,000
Market Share Assumptions			
FOCI	15%	10%	8%
Others (TFC, Corning, etc.)	80%	85%	85%
FAU ASP Assumptions			
FAU ASP (6.4T; US$)	220	220	220
FAU ASP (3.2T; US$)	100	100	100
FAU ASP (1.6T; US$)	45	45	45
FOCI Revenue contribution from NVIDIA			
Revenue contribution (US$mn)	9	186	597
Revenue contribution (NT$mn)	261	5,568	17,914
FOCI CY Revenue (NT$mn)	2,100	6,791	19,914
% of total revenue	12%	82%	90%

CPO Insertion Test Flow

Test Insertion	Insertion 1 (wafer-level)	Insertion 2 (wafer-level)	Insertion 3 (die-level)/3.5 (package-level)	Insertion 4 (module-level)		Insertion 5 (potential)
				Insertion 4O	Insertion 4E	
Test content	Electronic IC (EIC) & Photonic IC (PIC)	EIC die to PIC wafer (after SoIC)	Optical engine (die-to-die)	CPO package (ASIC+OE) Optical Testing	CPO package (ASIC+OE) Electrical Testing (2025-2026) Optical+Electrical Testing (starting 2027e)	CPO package (ASIC+OE) SLT?
Testing surface						
Key Product timeline	2025-2026 Scale-out CPO switch (Spectrum+Quantum) products 2027e onward: Scale-out CPO switch (Spectrum+Quantum) + Scale-up CPO switch products					
Testing details	El. & opt. DC, (power, loss, dark current etc.)	E/O, O/E, O/O, high speed, S-parameters	Full calibration/DC, high-speed functional, optical loopback, alternatively: S-parameters	Optical Light Transmission Testing, optical loopback	BER testing, signal testing	Full system functional validation
Testing service provider	Foundry (Wafer-level) TSMC	Foundry (Wafer-level) TSMC	OSAT (Die/chip level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)
Equipment and Consumable Vendo	PIC ATE tester: 1) Advantest + TEL + Formfactor 2) Chroma (underqualification) EIC tester: 1) Teradyne + TEL EIC Probe card: FormFactor	Wafer level testing: 1)Ficontec +Formfactor +Teradyne 2) Advantest+ **MPI**	Die-to-die prober: 1. TEL 2. MPI Optical engine E/O tester+laser reliability test+ELS source test head: Chroma **Optical and Electrical Test Socket: Winway**	CPO switch tester: Chroma **Hypersocket: Winway**	ATE tester: 1) Advantest (under qualification) 2)Teradyne **FT Handler+ELS source test head+optical alignmnet stage : Hon Precision** **Hypersocket: Winway**	CPO SLT tester: Chroma (under qualification) **Coaxial socket/Hypersocket: Winway**

Allring Benefited from CPO, New US Customers and Ongoing CoWoS Capacity Expansion from Non-TSMC

Allring Revenue Bottom-up Assumption

(NT$mn)	2024	2025	2026e	2027e	2028e	2025 Y/Y	2026 Y/Y	2027 Y/Y	2028 Y/Y
CoWoS	3,530	4,771	8,055	13,500	14,400	35%	69%	68%	7%
CPO	0	150	200	3,000	4,500	NA	33%	1400%	50%
Flip Chip	200	0	900	200	0	-100%	NA	-78%	-100%
SoIC		120	150	600	700		25%	300%	17%
US customer				200	200				
Others	1,804	325	750	500	800	-82%	131%	-33%	60%
Total Revenue	**5,535**	**5,366**	**10,055**	**18,000**	**20,600**	**-3%**	**87%**	**79%**	**14%**

Revenue mix	2024	2025e	2026e	2027e	2028e
CoWoS	64%	89%	80%	75%	70%
CPO	0%	3%	2%	17%	22%
Flip Chip	4%	0%	9%	1%	0%
SoIC	0%	2%	1%	3%	3%
US customer	0%	0%	0%	1%	1%
Others	33%	6%	7%	3%	4%
Total Revenue	**100%**	**100%**	**100%**	**100%**	**100%**

Quantum Security

Governments have established Post-Quantum Cryptography migration roadmaps

Exhibit 13: Migration timelines differ across regions, with 2030 as a key inflection point

United States	2027	Deprecate vulnerable cryptographic algorithms	2030	Complete migration of critical systems
European Union	2026	Publish migration roadmap	2030	Complete protection of sensitive information systems
United Kingdom	2028	Complete inventory and initial migration planning	2035	Full migration completed
South Korea	2028	Complete inventory and migration planning	2035	Complete migration of national cryptographic systems

Major economies are largely aligning with NIST PQC standards, while some countries continue developing domestic cryptographic frameworks.

Source: Topology Research Institute, Morgan Stanley Research

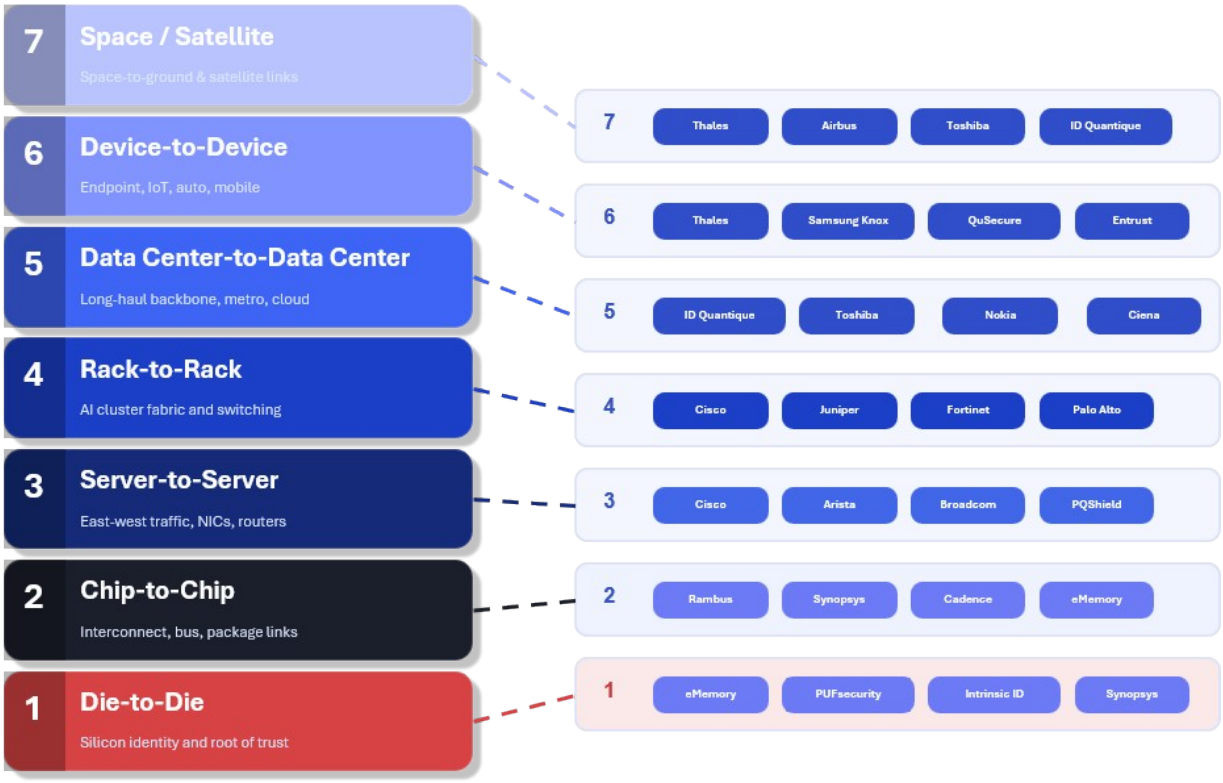
Asymmetric cryptography is the dominant security framework in modern electronic systems

Exhibit 21: Asymmetric encryption



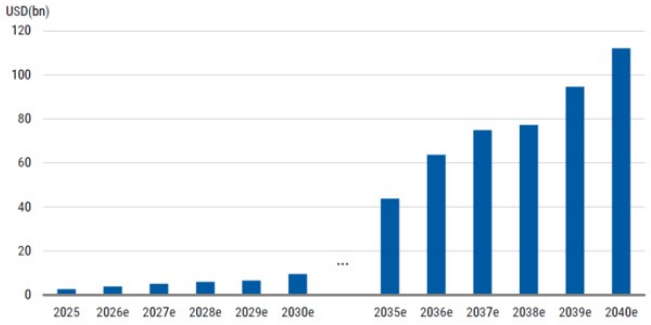
Source: cheapsslsecurity

Quantum security across different connectivity layers



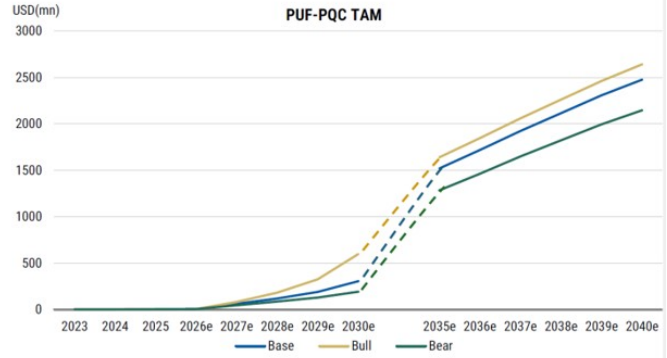
We estimate PUF TAM to be around US$310mn by 2030

Exhibit 1: We project the quantum infrastructure TAM will reach US$110bn by 2040



Source: Morgan Stanley Research (E) estimates.

Exhibit 3: The quantum hardware security TAM – our bull, base and bear cases



Source: Company data, Morgan Stanley Research estimates.

Global quantum supply chain – Hardware security is the foundation

