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Greater China Semiconductors

OCP Wrap-up: Rising Optics and AI Infrastructure Alternatives

Our US trip highlighted ICA/IPO traction, complementary rack-management silicon, hardware security and CXL-based memory pooling, with potential storage server upside.

Key Takeaways

- ICA/IPO traction: China CSP and TE demonstrations suggest growing adoption, although cost could be higher
- IMC versus BMC: Marvell IMC complements AST2700; we see no production disruption.
- Hardware security: Caliptra strengthens the case for eMemory PUF-based security IP.
- CXL and thermal: CXL supports memory pooling: Cooling and ASIC/CPU ramps remain in focus. Muse is likely driving storage server demand.

ICA/IPO: Gaining traction, but cost still a hurdle. A China CSP outlined optical form factors from XPO/NPO to interposer optics (IPO) and CPO, including integration of IPO with interposer copper attach (ICA). TE Connectivity showcased 224G/448G NPO/CPO sockets and ICA sockets with 0.4mm pitch and up to 10,000 pins, offering high-density connectivity, low crosstalk and improved reworkability. We see rising traction for ICA/IPO, with potential mass production in 2027 (For more, see our recent CPO report).

Marvell IMC: Complementary to AST2700, not a replacement. Marvell demonstrated the OCTEON-based infrastructure management controller (IMC) addresses higher-level AI rack/cluster telemetry and control; ASPEED's AST2700 BMC continues to handle node-level security and remote management. Given distinct functions and software ecosystems, we do not view IMC as a direct AST2700 competitor. We also don't see an AST2700 production issue, supporting an on-track ramp. The key debate is actually market share in TPU/Axion.

Caliptra: Expanding hardware Root of Trust opportunities. The open Caliptra framework defines silicon-level Root of trust (RoT) for data-center processors and accelerators, supporting secure boot, device identity and attestation eMemory (3529.TW) subsidiary PUFsecurity offers PUFrt, providing NeoPUF-derived device, NeoFuse OTP secure storage and hardware entropy as physical security building blocks for Caliptra implementations. Broader adoption could support incremental PUF/security-IP licensing, although monetization depends on qualifications and customer design wins. (For more, see our quantum security report).

Other: CXL fabric, cooling and compute ramps: The microchannel lid demonstration underscored the importance of chip-level thermal design as rack

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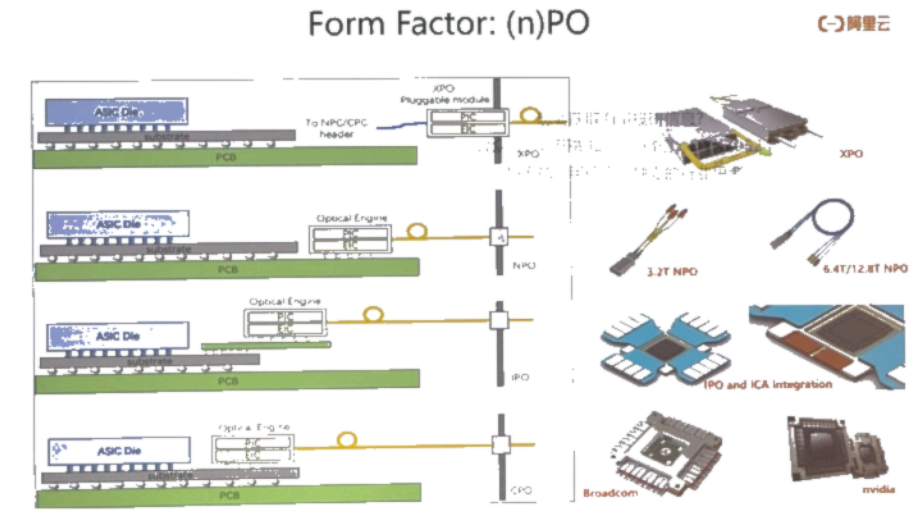
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density increases. The MARS demonstration with Partners underpins the importance of CXL fabric switches to connect multiple hosts with shared memory at rack scale, despite still taking time for maturity. Custom ASIC and server CPU ramps remain on track. Storage server demand could rise on Muse.

OCP – New optics solution?

Exhibit 1: Alternative optics solution: IPO



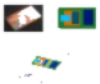
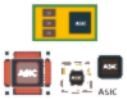
Source: OCP, Alibaba

Exhibit 2: ICA/IPO from TE



Source: TE

Exhibit 3: CPO Insertion Test Flow

Test Insertion	Insertion 1 (wafer-level)	Insertion 2 (wafer-level)	Insertion 3 (die-level)/3.5 (package-level)	Insertion 4 (module-level)		Insertion 5 (potential)
				Insertion 4O	Insertion 4E	
Test content	Electronic IC (EIC) & Photonic IC (PIC)	EIC die to PIC wafer (after SoIC)	Optical engine (die-to-die)	CPO package (ASIC+OE) Optical Testing	CPO package (ASIC+OE) Electrical Testing (2025-2026) Optical+Electrical Testing (starting 2027e)	CPO package (ASIC+OE) SLT?
Testing surface						
Key Product timeline	2025-2026 Scale-out CPO switch (Spectrum+Quantum) products 2027e onward: Scale-out CPO switch (Spectrum+Quantum) + Scale-up CPO switch products					
Testing details	El. & opt. DC, (power, loss, dark current etc.)	E/O, O/E, O/O, high speed, S-parameters	Full calibration/DC, high-speed functional, optical loopback, alternatively: S-parameters	Optical Light Transmission Testing, optical loopback	BER testing, signal testing	Full system functional validation
Testing service provider	Foundry (Wafer-level) TSMC	Foundry (Wafer-level) TSMC	OSAT (Die/chip level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)	OSAT (Die/package level) SPIL (ASE Group)
Equipment and Consumable Vendo	PIC ATE tester: 1) Advantest + TEL + Formfactor 2) Chroma (underqualification) EIC tester: 1) Teradyne + TEL EIC Probe card: FormFactor	Wafer level testing: 1)Ficontec +Formfactor +Teradyne 2) Advantest+ MPI	Die-to-die prober: 1. TEL 2. MPI Optical engine E/O tester+laser reliability test+ELS source test head: Chroma **Optical and Electrical Test Socket: Winway**	CPO switch tester: Chroma **Hypersocket: Winway**	ATE tester: 1) Advantest (under qualification) 2)Teradyne **FT Handler+ELS source test head+optical alignmnet stage : Hon Precision** **Hypersocket: Winway**	CPO SLT tester: Chroma (under qualification) **Coaxial socket/Hypersocket: Winway**

Source: Company data, Morgan Stanley Research (e) estimates