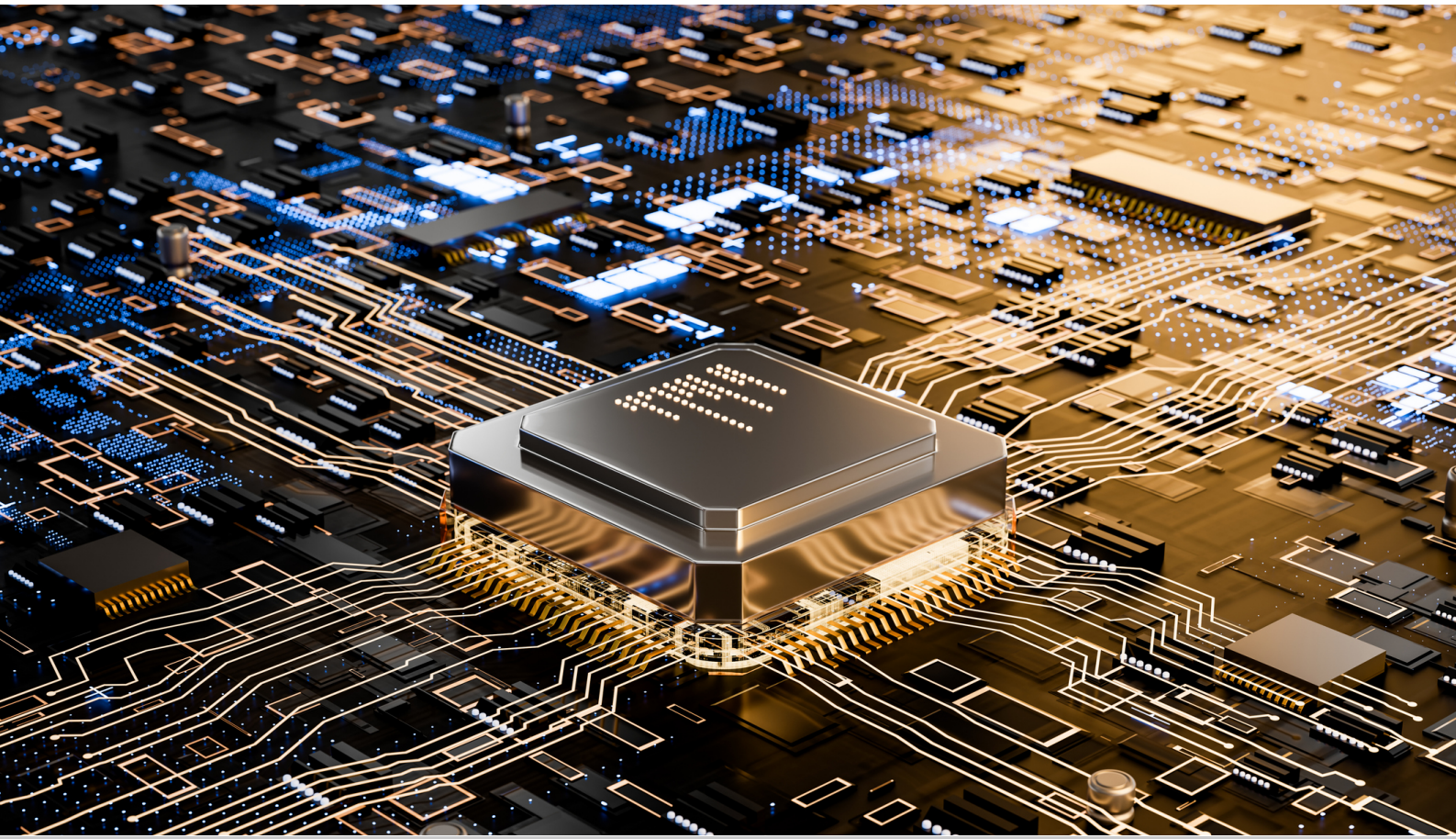
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ANCHOR REPORT

Global Markets Research

8 October 2026



AI data center power supply market

Development of new GPU power delivery networks and demand for passive parts

We compare and analyze the shift from lateral power delivery to vertical power delivery and IVR systems using simulations based on virtual processors.

- Methodology: We devised virtual processors equivalent to Nvidia's Blackwell and Rubin series and compared GPU power delivery network configurations using simulations.
- Comparison of power delivery systems: Lateral power delivery met our design criteria in the Blackwell-equivalent model but failed to do so in the Rubin-equivalent model, even with increased capacitance, and we had to relax the conditions. The use of vertical power delivery and integrated voltage regulator (IVR) systems improved power supply stability, and the IVR system met our design criteria. These systems use less capacitance on the output side of the voltage regulator but need more capacitance on the input side.
- Implications for passive parts: Increases in GPU power consumption are changing the configuration of electronic parts, the required capacitance, and where they are located. In future, we think embedding capacitors and making inductors smaller will be crucial.
- Stock picks: We recommend Murata Manufacturing for the comprehensive strengths of its broad product lineup, and TDK for its lead in thin-film inductors.

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See Appendix A-1 for analyst certification, important disclosures and the status of non-US analysts.

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AI data center power supply market

EQUITY: JAPAN ELECTRONIC PARTS

Development of new GPU power delivery networks and demand for passive parts

We compare and analyze shift from lateral power delivery to vertical power delivery and IVR systems using simulations based on virtual processors

Simulating power supply configurations based on virtual processors

We think the market for AI data center power supplies will present a wide range of investment opportunities. Power delivery networks (PDNs), which supply electricity to GPUs, are approaching a turning point in terms of designing the configurations of capacitors and voltage regulators as the power consumption of GPUs increases. In this report we carry out a simulation of virtual processors with the same electrical properties as Nvidia's Blackwell and Rubin products to compare and study PDN configurations for these virtual processors.

Comparing use of vertical power delivery and IVR systems versus lateral power delivery

We first built lateral power delivery models for both processors and calculated the split in current demanded by the GPU between voltage regulators and capacitors, as well as PDN impedance and voltage droop. We then constructed models for the Rubin-equivalent processor using vertical power delivery, where the voltage regulator is placed below the GPU, and for an integrated voltage regulator (IVR) system, where voltage regulation is integrated into the package. We compared these against lateral power delivery in terms of how improved voltage regulator responsiveness and shorter power delivery pathways affect voltage stability and capacitor configuration.

Qualitative changes in component configurations depending on power delivery system

The results of our simulations showed that the lateral power delivery model for our Blackwell-equivalent processor cleared our design criteria, but the Rubin-equivalent processor, which has higher power consumption, failed to achieve its target impedance with lateral power delivery, and we needed to relax our load fluctuation condition. Even after this, the effective capacitance on the output side was some 60% higher than for the Blackwell-equivalent processor (roughly 32mF). Increasing capacitance on the PCB side had little impact, and the only effective measure was increasing capacitance within the package, close to the GPU. By contrast, the improved voltage regulator responsiveness and shorter power delivery pathways in the vertical power delivery and IVR systems improved voltage stability. The IVR model met our design criteria, and impedance in the vertical power delivery model only exceeded the tolerable maximum by around 2%. The shorter power delivery pathways also reduced power distribution losses caused by resistance. The effective capacitance on the output side of the voltage regulator fell to around 13mF in vertical power delivery and around 1.8mF in IVR, but more capacitance was needed on the input side. The higher the voltage of input-side rails, the lower the capacitance required. This shows that increased GPU power consumption will not just simply boost capacitor demand in terms of capacitance but have a qualitative impact on part types, capacitance, and mounting locations. Given the limited mounting area provided by packages, we think moves to embed capacitors and increase mounting density will be crucial, alongside inductors to help make voltage regulators smaller.

We recommend Murata Manufacturing for comprehensive capabilities, TDK for leading position in thin-film inductors

We recommend Murata Manufacturing [6981] and TDK [6762] as companies likely to benefit from these advances in PDNs. Murata Manufacturing's strength lies in its broad product lineup that can keep up with changes in power delivery systems, including compact, high-capacitance MLCCs for lateral power delivery, Integrated Package Solution (iPaS) products for vertical power delivery, and silicon capacitors for IVR systems. TDK has strengths in thin-film inductors that we expect to be used in vertical power delivery and IVR systems, and it has also been working on the development of high temperature-rated MLCCs, which we think will be increasingly used in PDNs.

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Introduction

Looking for investment opportunities in market for AI data center power supplies

We think the market for AI data center power supplies will present a wide range of investment opportunities. Power supply to data centers is broadly divided between power distribution, which refers to getting electricity to the racks, and power delivery networks (PDNs), which take the electricity supplied to the racks and step the voltage down so that it can be used by the processors.

Two power supply markets: Power distribution and PDN

Power distribution systems have been shifting to higher voltages to deliver more power closer to the load and to reduce both current and power losses. PDNs take the high-voltage power delivered to the rack and step it down to 1.0V or lower close to the GPU, and are seeing a shift towards shorter low-voltage, high-current wiring sections.

PDN market: Supplying power to GPU using voltage regulators and capacitors

The power required by a GPU is not consistent but varies widely in a short space of time depending on the operating state of compute units and memory. Different components are used to deal with these fluctuations in load, with capacitors close to the GPU, capacitors in package or on the PCB, and voltage regulators supplying power in different time windows depending on their responsiveness. Capacitors close to the GPU make up for current shortfalls immediately after a surge in load, and high-capacitance capacitors and voltage regulators that are more distant take over power supply after that. Generally speaking, capacitors closer to the GPU provide less energy but can deal with faster changes in load. By contrast, more distant capacitors and voltage regulators can supply more energy but it takes longer for them to get the current to the load because of the resistance of the wires and loop inductance.

Shift in voltage regulators from lateral power delivery to vertical power delivery and integrated voltage regulators

This means that ensuring stable power supply to GPUs requires an integrated design approach that factors in voltage regulator responsiveness and capacitor placement not only to ensure the necessary capacitance in the capacitors but also to get the energy required to the GPU when it is needed. In particular, increasing fluctuations in GPU power consumption and load current can make it more difficult for lateral power delivery, the current mainstream type of PDN, to respond just by raising the number of capacitors and increasing voltage regulator responsiveness. Notable solutions to this issue are technologies to shorten the power supply path itself, such as vertical power delivery, where the voltage regulators are sited directly below the GPU, and integrated voltage regulator IVR), where voltage regulation happens on-package.

Construction of simulation models using virtual processors

In this report we construct a simulation model for PDNs that can respond to the power requirements of virtual processors that have the power characteristics of Nvidia's Blackwell and Rubin products (Blackwell: power consumption of 1,000W and core voltage of 0.75V, Rubin: power consumption of 2,300W and core voltage of 0.70V). We use these models to analyze the conditions required in power supply for future high-performance processors rather than to reproduce the internal circuitry and components used with actual Nvidia products.

Time window model of capacitor/voltage regulator supply of GPU required current

In our simulation, we look at whether the voltage regulators and capacitors can cope with the current required by the GPU and whether the system can keep the voltage at the processor terminals within the tolerable range. Voltage regulators cannot immediately keep up with rapid changes in GPU load, and capacitors are used to make up for the interim current shortfalls. Here, we look at capacitor charge swing, defined as the variance in electrical charge over the charging cycle of the capacitor resulting from the difference between current demanded by the GPU and current supplied by the voltage regulator (measured in coulombs), and look at how it affects changes in voltage. We also look at the energy buffer, defined as the energy that capacitors can supply to the GPU during periods of change in load to ensure that the voltage remains within its tolerable range (measured in joules), and see whether it can fully support the GPU requirements.

We use these evaluations to come up with capacitor requirements (measured in farads) and mounting configurations that can keep voltage swings within the tolerable range, factoring in wiring resistance, loop inductance, and voltage regulator responsiveness.

First assumptions are for Blackwell- and Rubin-equivalent lateral power delivery

We first construct a lateral power delivery model for Blackwell- and Rubin-equivalent processors, and analyze how higher GPU power consumption affects PDN design criteria. Using a strict load-step condition (ΔI) with the Rubin-equivalent processor pushes the impedance of the lateral power delivery model above the upper limit (target impedance) needed to keep voltage swings within the tolerable range, and resolving this requires either easing the load-step condition, sharply increasing capacitor count, or increasing voltage regulator responsiveness. Having identified these design constraints, we compare voltage stability and the required energy buffer in models that assume vertical power delivery or integrated voltage regulators.

Potential impact of using vertical power delivery or integrated voltage regulators

We use this information to analyze potential changes to the energy buffer needed between the input and output sides of the voltage regulator from the shift in power supply design to vertical power delivery or IVR, thereby providing insight into how this will affect future capacitance requirements, capacitor mounting location, and product mix, as well as demand for related parts and materials.

1. AI data center power supply configuration and GPU power delivery

AI data center power supply configuration

AI accelerators consist of multiple compute units running in parallel, which means PDNs have to both supply of large currents at low voltage and respond to sudden changes in load. Understanding the mechanisms that can support these power requirements can give us an insight into how power supplies for AI data centers are configured.

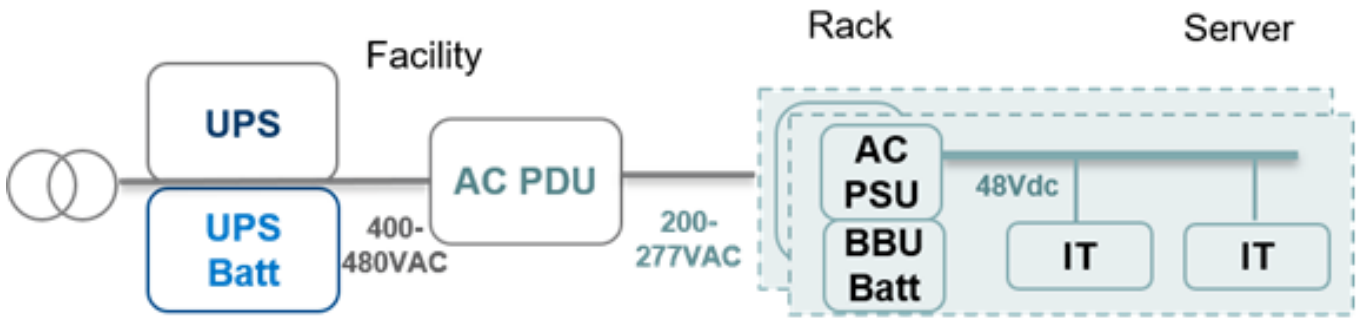
Power distribution: Supplying 480V AC to server racks

AI data centers take the medium-voltage (MV) alternating current (AC) provided by electric power companies and use transformers to step it down to 400V or 480V. From here, the power is supplied to the rack enclosures via automatic transfer switches (ATSs), uninterruptible power supplies (UPSs), and power distribution units (PDUs).

Rack enclosure: Stepping down from 480V AC to less than 1V

Within the rack enclosure, power supply units (PSUs) on power shelves are used to convert this current to nominal 48V DC (50–54V in real terms), which is then distributed to the server units via busbars. In the server units, this is then stepped down to intermediate voltage using DC-DC converters such as intermediate bus converters (IBCs) as needed, and the final voltage regulators then step this down to the GPU's core voltage of 1V or less (Figure 1). Voltage regulators adjust the supplied current by monitoring the output voltage and ensuring that the voltage remains within a given range (however, they cannot immediately respond to sudden changes in load, and capacitors have to be used to provide current shortfalls).

Fig. 1: AI data center power supply configuration



Source: Nomura, based on Schneider Electric, Delta data

48V DC power supply buses are current mainstream for rack enclosures

Conventional servers frequently use PSUs within the server unit to convert 200V AC to 12V DC. In 48V power supply systems, the conversion to DC is centralized in the power shelf at the rack level, and then distributed to the server units using a common 48V-class busbar. A higher voltage allows the same power to be delivered at a lower current, thereby reducing the power distribution losses in the busbar and connectors. 48V buses are connected to battery backup units (BBUs) to ensure ongoing power supply over a certain period of time even if the AC input is lost.

We analyze power supply from PDN voltage regulators through to GPU

In this report we define power distribution as everything from MV input through to just before 48V DC conversion in the PSU (the AC input side) and the power distribution network (PDN) as everything from the 48V DC output of the PSU through to the AI accelerator. The PDN includes the 48V bus, IBCs, which are installed as needed, and final-stage voltage regulators, capactors, and wiring.

Here, the main targets of analysis in our simulation are the final-stage voltage regulators, the capacitors on the input and output sides of this, and the wiring, while upstream, one-time voltage conversion parts, such as the power shelf and the 48V bus, fall outside the scope of our analysis. We estimate voltage regulator output current and capacitor charging/discharging current over time in response to changes in GPU load and use this to evaluate energy allocation and voltage changes for different time windows. Based on this, we identify the roles of the voltage regulators and capacitors in each different power supply method and also use determine the required capacitance of capacitors on both the input and output sides via simulation.

Electrical energy characteristics required by GPUs

GPUs achieve their high compute performance by operating multiple compute units and on-chip memory in parallel. Large-scale AI GPUs operate these circuits at high activity rates, which means they require the supply of average current of several thousand amps at low voltages.

Moreover, the compute units and memory repeatedly switch between active and idle states depending on what processing they are doing, resulting in a load current that is not constant. The current increases sharply when multiple circuits start calculations or data transfer at the same time, and then falls when the processing is complete. As these changes occur at intervals measured in nanoseconds, GPU PDNs require the ability to both supply power continuously at with a high average current and to respond to sudden changes in step-load (large ΔI).

Electrical energy supply to GPU

The voltage regulator constantly supplies electrical current to the GPU and adjusts the output according to changes in load. However, the control circuitry has a response time, and it cannot change the current flowing through the output inductor of the voltage regulator instantly. Because of this, capacitors placed close to the GPU are used to supply the missing current immediately following a sharp increase in load, while in the interim the voltage regulator increases the supply current and then takes over the load. When the load declines, the capacitors absorb the spare current (in a charge cycle) to curb any increase in voltage.

Role of inductors and capacitors in PDNs

Capacitors help reduce voltage fluctuations by absorbing or releasing the load, while inductors prevent sharp fluctuations in current flow. Step-down voltage regulators smooth out the current using inductors, but their characteristics limit the take-off of current when the load rises sharply. Capacitors can make up the shortfall until the voltage regulator output can catch up with the load.

Target impedance set during power supply design stage

Designing a GPU power supply requires maintaining supply voltage within a tolerable range even if the load current varies. Here, impedance (measured in ohms) is the quantity that expresses how much the voltage fluctuates in response to changes in current, and voltage fluctuation is determined as change in current multiplied by impedance. The target impedance is defined as the tolerable fluctuation in voltage divided by the maximum fluctuation in load current, and the basis of the design is to keep the impedance of the PDN as a whole below this level. The greater the fluctuations in load current, the lower the impedance required to keep voltage within the same range. There are two ways to



reduce impedance. The first is to increase capacitance, but because the capacitors themselves and the connecting wiring have inductance, there is no reduction in impedance even if capacitance (versus rapid changes in current) is increased in the high frequency domain, meaning limited impact. The other is to reduce inductance of the pathways carrying power (so-called loop inductance).

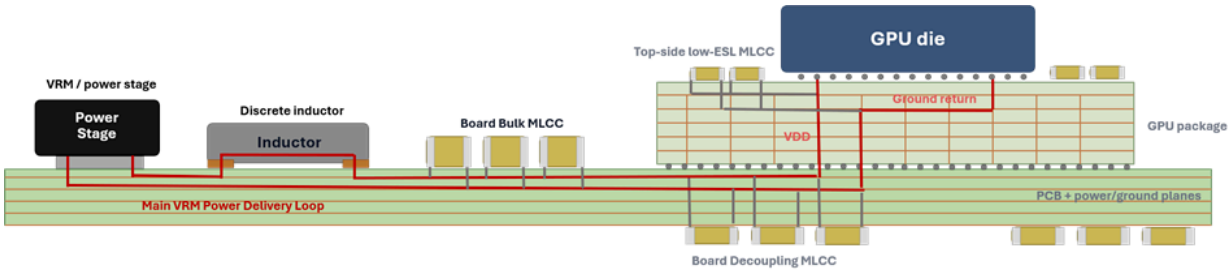
Reducing voltage below base value can cause GPU instability

If the impedance of the PDN exceeds the target level, it can cause a decline in voltage (known as voltage droop) beyond acceptable limits when the load increases sharply. An excessive decline in voltage could destabilize the operation of the GPU, causing lower compute performance, calculation errors, or operational halts, which makes keeping voltage droop and PDN impedance within the tolerable range across the relevant frequency bands a crucial part of PDN design.

Diagram of loop inductance in lateral power delivery

Figure 2 shows a diagram of the current loops and capacitor placement in GPU power supplies that use lateral power delivery. When the GPU load increases, current is supplied to the GPU not only from voltage regulators but also from capacitors on the board and located close to the GPU. Here, the current flows on the supply side from the capacitors to the GPU and then back to the capacitors via the ground side. In other words, the current forms a closed loop with an outward path and a return path. Loop inductance is then defined as the total inductance of all the wiring, vias, power supplies, ground planes, and other parts of the loop. The greater the loop inductance, the longer it takes for current to rise, causing bigger voltage swings at the GPU terminal.

Fig. 2: Current loop in GPU PDN using lateral power delivery voltage regulators



Source: Nomura

Capacitor placement needs to match time window

The closer a capacitor is to the GPU, the shorter the current path, and, generally speaking, the lower the inductance is likely to be. By contrast, the current path from voltage regulators and capacitors placed at some distance away on the PCB is longer, which means a greater impact from wiring resistance and loop inductance. This means that capacitors not only have to have the right amount of energy stored but have to be placed in a location where they can deliver that energy to the GPU when required. It is particularly important in AI GPUs to ensure short outward and return paths by placing capacitors within the package or on the board backside directly below the GPU.

Capacitor and voltage regulator placement by time window

Figure 3 shows where capacitors and voltage regulators are positioned in GPU PDNs and the main time windows where they are used. Current is primarily supplied by on-die capacitance in the first 10ns or so immediately after a surge in load, and then by MIM and silicon capacitors within the package or MLCCs (DSCs and LSCs) in the following 10–100ns. Over the next few microseconds, the MLCCs located directly beneath the GPU make up for the shortfall until the supply current from the voltage regulators can catch up with the load, at which point the voltage regulators take over current supply for the subsequent time windows. These time windows are not clearly separated, and multiple capacitors and voltage regulators are used simultaneously to supply current. The time windows per component shown in Figure 3 are based on the results of the simulation in the following chapter, and should not be viewed as generalizations as they are likely to change depending on power supply design conditions.

Fig. 3: Time windows and locations for capacitors and voltage regulators (Current contributions based on simulation results)

Placement	Capacitors/voltage regulators	Placement	Loop inductance (relative)	Loop inductance (benchmark)	Ultrahigh speed			Fast (150ns)			Medium (1µs)		Slow (10µs)		Notes (role)
					0–1 ns	1–3 ns	3–10 ns	10–30 ns	30–100 ns	0.1–0.3 µs	0.3–1 µs	1–3 µs	3–10 µs	10–30 µs	
On GPU die															
	On-die capacitance	On die (transistor/wiring layers)	1	■□□□□ Very small (on die)											Local supply to make up for initial current shortfall
In package															
	MIM	Thin-film capacitors on package substrate	1	■□□□□ Very small (less than 1pH)											High-frequency decoupling of shortest package path, distributed placement required because of limited effectiveness of individual capacitors
	Silicon capacitors	In package, close to IVR output	2	■■□□□ Small (up to 10pH)											Primarily for transient response of less than 100ns (largely interchangeable with DSCs), strengths lie not only in area efficiency but also space savings from embedding, very low ESL, and no DC bias degradation
	DSC	MLCCs on top of package (die-side)	2	■■□□□ Small (less than 1pH)											Package MLCCs close to die (overlaps in function with silicon caps in IVR configurations, MLCCs have better capacitance per mounting area than silicon caps)
	LSC	MLCCs on bottom of package (land-side)	3	■■■□□ Small-medium (up to 10pH)											Package MLCCs at more distance from die
PCB															
	MLCCs below GPU	PCB backside, below GPU	3	■■■□□ Medium (10–100pH)											Primary medium buffer directly below GPU
	Peripheral MLCCs	PCB topside, near GPU	4	■■■■□ Large (up to 1nH, through voltage regulator path)											Assists in slow areas from voltage regulator side (charging/discharging on voltage regulator output side)
	Voltage regulator output polymer capacitors	Voltage regulator output side (SP-Caps etc)	5	■■■■■ Large (nH level)											Little role in supplying net charge to load transients, role is for charge exchange and smoothing on voltage regulator side
Voltage regulator (by supply type)															
	Lateral power delivery voltage regulators	PCB topside, next to GPU	5	■■■■■ Maximum (path: up to 1.2nH + output inductance)											Continuous supply of load current from PCB near GPU (TLVR boost makes up for low Kp/Ki, ensuring effective response speed)
	Vertical power delivery voltage regulators	PCB backside, below GPU	4	■■■■□ Large (path: up to 0.4nH + output inductance)											Continuous supply of load current from PCB below GPU for short loop
	Integrated voltage regulators (IVRs)	In package, close to die	3	■■■□□ Medium (path - 0.05nH, high-speed control)											Continuous supply of load current from within package near die for ultra-short loop, development focusing on phase inductors with dramatically reduced L/ESR (1/10 L, 1/4 ESR vs lateral) and multiphase miniaturization via coupled TLVR to keep up with rising GPU current transients

Note: (1) Current contribution is calculated as the net charge supplied by each source in each time window divided by the total charge supplied within that window. (2) We filter out capacitors with current contributions below a minimum threshold (default of 10%) to exclude those with small capacitance and thus make no material contribution during long time windows (for example, on-die capacitance that can output current in 1µs but has a current contribution of less than 1%).
Source: Nomura

2. PDN simulation model

Examining constraints in PDN design for Rubin-equivalent virtual processor

In this chapter we build a PDN simulation model for virtual processors with the same electrical characteristics as Nvidia's Blackwell and Rubin processors, and use this to analyze the impact of higher power consumption and changes in power delivery system on power supply performance and capacitor configuration. First, we compare lateral power delivery models for both processors and examine the design constraints from increased power consumption in the Rubin-equivalent processor. We then analyze the changes in power supply performance and capacitor configuration from moving to vertical power delivery and IVR systems.

We set basic 50% load-step condition in simulation

Simulations use a so-called step-load condition, which represents changes in current required over a short period of time, to replicate changes in GPU load. The step-load condition shows the extent of short-term changes in current demanded by the GPU (ΔI). In our model, we use a step-load condition of 50%, which is defined as a variation in current equivalent to 50% of peak current. The bigger the variation, the more current has to be provided by capacitors until the voltage regulators can catch up with the load, and the lower the target impedance required by the PDN. Figures 17 and 18 show at the end of this report show detailed design criteria. The simulation process is as follows.

Generating GPU current demand waveform

The first step is to create the GPU current demand waveform. We defined the average load current using specs from disclosure materials, such as the GPU's power consumption, and made assumptions for core voltage, load variation magnitude, rise time, and duration. From these criteria, we generated a time-domain load current waveform and input it into the simulation as the conditions that the voltage regulators and PDN must follow.

Calculating voltage regulator and capacitor response in time domain

Second, we calculated the response of the voltage regulators and capacitors to the GPU current demand waveform in the time domain. Voltage regulator output current cannot keep up with immediate changes in GPU current demand because of factors such as the response time of control circuits and inductance. Because of this, capacitors are used to make up for the shortfall in current in the immediate wake of a rise in load, and the need for using these capacitors declines at voltage regulator output current catches up. Meanwhile, surplus current when the load declines is used to charge the capacitors. We calculated not only this division of current between voltage regulators and capacitors but also the energy supplied by the capacitors on the voltage regulator input side when the load changes.

Calculating energy held by capacitors by time window

Third, we calculated the energy stored by the capacitors for each time window. We calculated the difference between GPU power demand voltage regulator power supply as capacitor charge swing (change in energy). In this report we call the energy stored temporarily in a capacitor to cope with these variations and to be supplied as required the energy buffer. We then calculated the effective capacitance required to secure the necessary energy buffer within the tolerable voltage range.

Estimating voltage stability using impedance and voltage droop

Fourth, we examined voltage stability by calculating PDN impedance and voltage droop. Our design criteria ensure that PDN impedance meets the set upper limit and that processor terminal voltage variations stay within the acceptable range, based on wiring resistance from the voltage regulators and capacitors to the processor, loop inductance, and voltage changes from capacitor discharge. Because the power supply path from capacitor to processor differs by mounting position, irrespective of capacitance, there will be differences in current that can be supplied in a short space of time and in voltage droop too. In view of this, we assessed capacitors not only in terms of capacitance but also referencing changes power delivery pathway resistance and inductance depending on mounting location.

Finding capacitor configuration that meets requirements

Fifth, we looked for capacitor configurations that would meet both electrical requirements and mounting criteria. We examined configurations that could ensure the required effective capacitance by varying the type, size, and number of capacitors while considering constrains such as the decline in capacitance caused by DC bias and mounting area. We then adjusted for voltage regulator responsiveness and power supply pathways to find configurations that meet our criteria for PDN impedance and voltage droop. In this way we obtained PDN configurations that can supply the required energy to the processor at the right time.

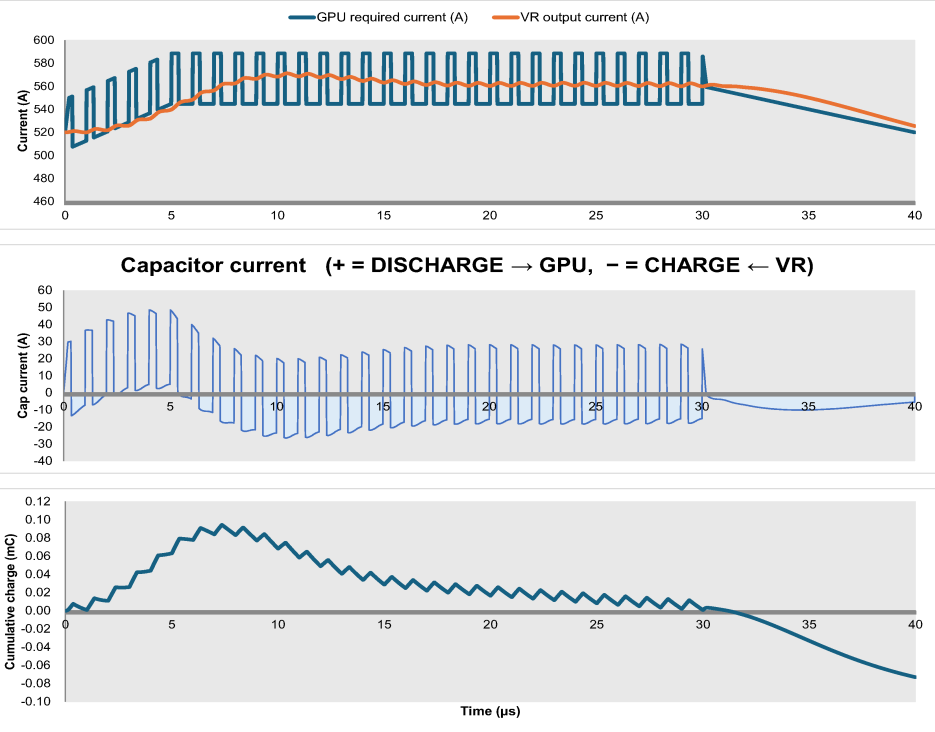
Comparison of Blackwell and Rubin simulation models

We used the simulation model described here to first compare the current split between voltage regulators and capacitors and voltage stability in lateral power delivery systems for Blackwell- and Rubin-equivalent virtual processors. In both simulations we applied a step-load condition of 50% (a 50% increase over the reference GPU current demand) and investigated how this increase in power demand affects PDN design criteria.

GPU demand current, voltage regulator output current, capacitor charge/discharge

Figure 4 shows current demand, voltage regulator output current, capacitor charge/discharge current, and cumulative charge over time for the Blackwell-equivalent model.

Fig. 4: Power demand, voltage regulator output, and capacitor charge/discharge in Blackwell-equivalent model



Source: Nomura

Capacitors used to fill in for instantaneous changes in current that voltage regulators cannot cope with

When GPU current demand rises sharply, output current from the voltage regulator cannot keep up, and capacitor discharge is used to make up for the shortfall. After that, the need to use these capacitors declines as supply current from the voltage regulator increases. By contrast, when the current demand declines, the supply current from the voltage regulator exceeds the load for a time, and this surplus current is used to charge the capacitors. The result of this repeated charge and discharge cycle is that the cumulative charge of the capacitor varies within a specified range.

Blackwell-equivalent model clears criteria

In our Blackwell-equivalent model, the combination of voltage regulators and capacitors ensures that PDN impedance and voltage droop remain within the set tolerable range even under the 50% load-step condition.

Rubin-equivalent model requires stricter impedance criteria when power increases

By contrast, our Rubin-equivalent model sees a rise in average load current when GPU power consumption increases, resulting in a greater current variability under the same 50% load-step condition. This means an increase in current that has to be made up for with capacitors and lower target impedance to ensure that voltage variability remains within the acceptable range. Figure 5 shows PDN impedance and design-based upper tolerable limits for both models.

Fig. 5: Comparison of lateral power delivery in Blackwell- and Rubin-equivalent models: PDN impedance (Z) and tolerable maximum (50% step-load condition)

Item	Blackwell-equivalent	Rubin-equivalent
Step-load condition	50%	50%
Target impedance	0.119	0.036
Tolerable maximum impedance (mΩ)	0.178	0.054
Minimum Z peak identified through optimization (mΩ)	0.178	0.092
Combined Droop（mV）	19.3	- (note 4)
Output-side effective capacitance (mF)	20.0	- (note 4)
Verdict	Compatible	Incompatible (assuming fixed configuration in package)
Upper limit overshoot (%)	None (matches upper limit)	Around 70%

Note: (1) The tolerable maximum impedance is set at 1.5x the target impedance. (2) Output-side effective capacitance is the capacitance of the capacitors on the output side of the voltage regulator designed to maintain the energy buffer needed to cope with fluctuations in load within the tolerable voltage range. (3) The Rubin-equivalent model has greater fluctuation under the base step-load condition of 50% than the Blackwell-equivalent model because of increased power demand, resulting in a fall in target impedance to about one-third of Blackwell. (4) The values for the Rubin-equivalent processor are the result of investigations based on 300 capacitors in the package (majority 0603). Under these conditions, the 50% step-load condition cannot be met with increases in capacitance below the GPU or on the output side of the voltage regulator alone. The step-load condition was met by increasing the capacitor count in the package to 525 at 1608 size (Z peak of 0.0541mΩ, output-side effective capacitance of 37.3mF, combined droop of 15.4mV). However, this would require a roughly 6.8-fold increase in mounting area within the package, and we did not investigate the feasibility of this. (5) In this report, we assume a set configuration within the package and use a lateral power delivery configuration for the Rubin-equivalent processor with the step-load condition relaxed to 30%. Note that this is not the same condition as for the Blackwell-equivalent processor.
Source: Nomura

Load-step condition not met in Rubin-equivalent model

Our simulation showed that the design criteria was met in our Blackwell-equivalent model, as noted earlier. By contrast, the PDN impedance in the Rubin-equivalent model exceeded its tolerable maximum. This means that retaining the lateral power delivery configuration to deal with rising power consumption in the Rubin-equivalent model would make it difficult to respond to a strict step-load condition (50%) without major improvements in capacitor capacitance and positioning, voltage regulation responsiveness, and power delivery pathways.

Examining impact of easing load-step condition

In view of this, we looked at the impact of easing the load-step condition in lateral power delivery for the Rubin-equivalent model. Figure 6 shows the results of changing the load-step condition to 50%, 35%, and 30%.

Fig. 6: Comparison of step-load conditions for lateral power delivery in Rubin-equivalent model

Item	Step-load condition		
	50%	35%	30% (adopted)
Target impedance	0.036	0.052	0.060
Tolerable maximum impedance (mΩ)	0.054	0.077	0.090
Minimum Z peak identified through optimization (mΩ)	0.092	0.090	0.090
Combined Droop (mV)	- (note 4)	- (note 4)	18.1
Output-side effective capacitance (mF)	- (note 4)	- (note 4)	31.5
Verdict	Incompatible (note 4)	Incompatible (note 4)	Compatible
Upper limit overshoot (%)	Around 70%	Around 16%	-0.6% (below maximum)

Note: (1) The tolerable maximum impedance is set at 1.5x the target impedance. (2) Output-side effective capacitance is the capacitance of the capacitors on the output side of the voltage regulator designed to maintain the energy buffer needed to cope with fluctuations in load within the tolerable voltage range. (3) The minimum Z Peak shows the minimum vale found through optimization processes for the 50% and 35% step-load conditions, and the value in the adopted configuration for the 30% step-load condition. (4) The incompatible findings for 50% and 35% assume a fixed configuration in the package of 300 capacitors (majority 0603). Increasing the package size and capacitor count would result in criteria being met even with lateral power delivery. The criteria are met at the 35% step-load condition with a configuration of 300 1608 capacitors (Z peak of 0.0706mΩ, effective capacitance of 35.3mF, combined droop of 17.0mV) and at the 50% step-load condition with a configuration of 525 1608 capacitors (0.0541mΩ, 37.3mF, 15.4mV). However, these would require roughly 3.9-fold and 6.8-fold increases in mounting area within the package respectively, and we did not investigate the feasibility of these configurations.
Source: Nomura

Reducing step-load condition to 30% finally results in clearance

The 50% step-load criteria results in impedance exceeding its upper bound substantially, and even reducing this to 35% does not allow it to meet the design criteria. However, easing it to 30% keeps impedance below its acceptable maximum, resulting in a successful outcome for the lateral power delivery model. However, this means little leeway versus the upper bound, and still represents stringent design criteria.

Using 30% in Rubin-equivalent lateral PDN model

In view of this, below we use a configuration that meets the 30% load-step condition as the model for lateral power delivery for the Rubin-equivalent processor. This 30% figure does not represent the actual load fluctuation characteristics of Nvidia's Rubin processors but is a simulation condition needed to fulfill the PDN model design requirements we set.

Barriers to improving performance in lateral power delivery

As our model shows, continuing to use lateral power delivery to meet the power consumption requirements of the Rubin-equivalent processor requires easing the step-load condition or improving performance of the PDN through a combination of greatly increasing the number of capacitors and increasing the responsiveness of voltage regulators. That said, increasing the number of capacitors is constrained by mounting surface area, and even if voltage regulator responsiveness is improved, performance will still be affected by the resistance of the supply pathways to the GPU and loop inductance.

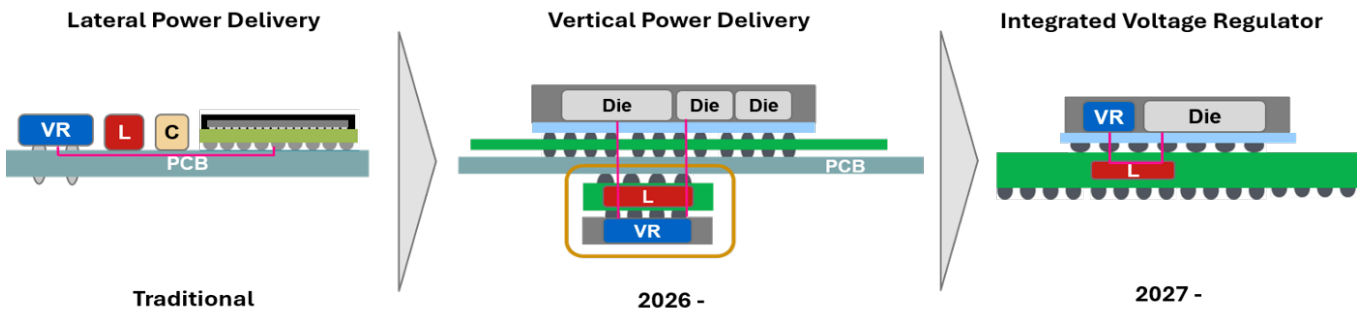
We next look at impact of using vertical power delivery and IVR systems

In this next section, we look at using vertical power delivery and IVR systems, which reduce the length of the supply pathways from the voltage regulators to the GPU, and examine voltage stability and capacitor energy sharing under a 50% step-load condition for the Rubin-equivalent model.

Simulation using vertical power delivery and IVR systems

Under the Rubin-equivalent lateral power delivery model, we have to greatly increase capacitor numbers or improve voltage regulator responsiveness to cope with stringent step-load conditions. Here, we carried out simulations for vertical power delivery, where the voltage regulator is positioned below the GPU, resulting in a shorter, vertical electrical pathway than under the lateral configuration, where the pathway flows laterally across the board surface, and IVR, where the pathway is shortened by integrating voltage regulation inside the GPU package. Figure 7 shows diagrams of both systems.

Fig. 7: Schematic of lateral power delivery, vertical power delivery, and IVR systems



Source: Nomura, based on TDK data

Comparing power supply performance of different configurations

First, we applied a 50% step-load condition to the Rubin-equivalent processor and compared the impact of the different power delivery configurations on PDN impedance and voltage droop (Figure 8).

Fig. 8: PDN performance and output-side effective capacitance by power delivery system in Rubin-equivalent model (50% step-load condition)

Item	Lateral power delivery	Vertical power delivery	IVR
Step-load condition	50%	50%	50%
Tolerable maximum impedance (mΩ)	0.0542	0.0542	0.0542
Minimum Z peak identified through optimization (mΩ)	0.092	0.0552	0.0449
Combined droop (mV, target 35.0)	- (note 1)	14.81	14.41
Output-side effective capacitance (mF)	- (note 1)	13.1	1.77
Verdict	Incompatible (note 1)	Conditionally compatible	Compatible
Overshoot versus maximum	roughly +70% (undershoot)	Around 2%	-17% (leeway)

Note: (1) Figures for lateral power delivery assume a fixed capacitor configuration within the package (minimum Z peak of 0.092mΩ). Increasing the capacitor count within the package to 525 of 1608 size fulfills the 50% step-load condition (Z peak of 0.0541mΩ, effective output-side capacitance of 37.3mF), but would require a roughly 6.80-fold increase in mounting area within the package. The vertical power delivery and IVR systems bring the voltage regulator closer to the GPU, which solves the constraints without increasing capacitor count within the package. (2) Vertical power delivery meets the criteria with conditions, with an overshoot versus the tolerable maximum impedance of roughly 2%, while IVR meets the criteria, coming in some 17% below the maximum. (3) IVR meets the criteria thanks to its shorter power delivery pathway, which reduces loop inductance and wiring resistance, allowing the voltage regulator to operate stably at a higher bandwidth.
Source: Nomura

Sharp improvement in power supply performance

Whereas lateral power delivery resulted in impedance greatly exceeding its upper bound at the 50% step-load condition, the overshoot with vertical power delivery was reduced to only around 2%, and the use of IVR resulted in the design criteria being met. Vertical power deliver showed a major improvement in power supply performance versus lateral power delivery, even if it did not strictly meet the upper bound.

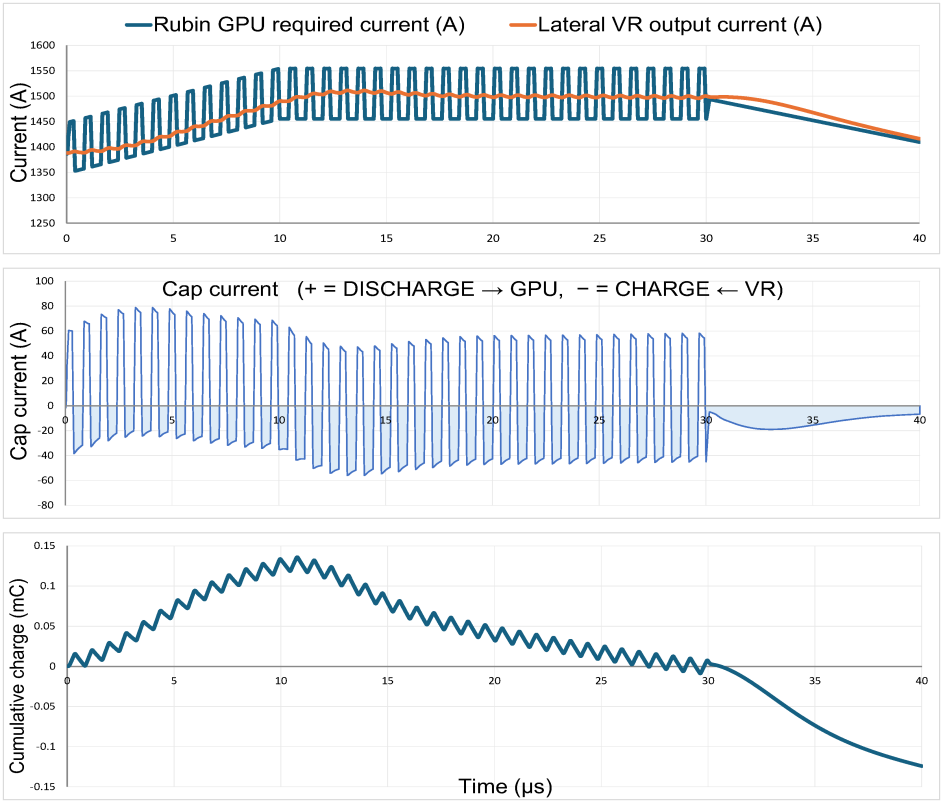
Shortening pathway from voltage regulator to GPU is key

These results show that the importance of shortening the electrical pathway from the voltage regulator to the GPU and increasing the responsiveness of the voltage regulator to get the required current to the processor quickly as a means of coping with sharp fluctuations in load. Note that in the current model, we use a 30% step-load condition to meet the criteria with lateral power delivery but use a 50% condition for vertical power delivery and IVR. Accordingly, readers should remember that the comparisons between models below use different step-load conditions.

Current sharing between voltage regulators and capacitors

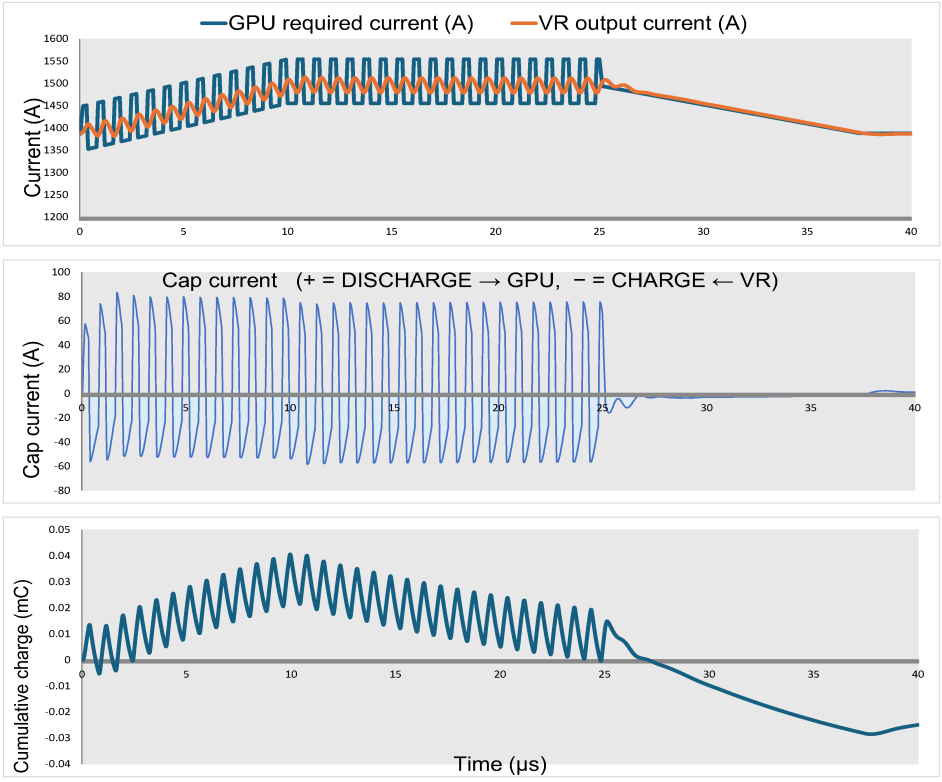
Next, we looked at current sharing between voltage regulators and capacitors to get an insight into the differences in power supply performance for these different configurations. Figures 9–11 show GPU current demand, voltage regulator output current, capacitor charge/discharge current, and cumulative charge over time for all models.

Fig. 9: Capacitor charge/discharge and voltage regulator output in response to charge request in Rubin-equivalent model (lateral power delivery)



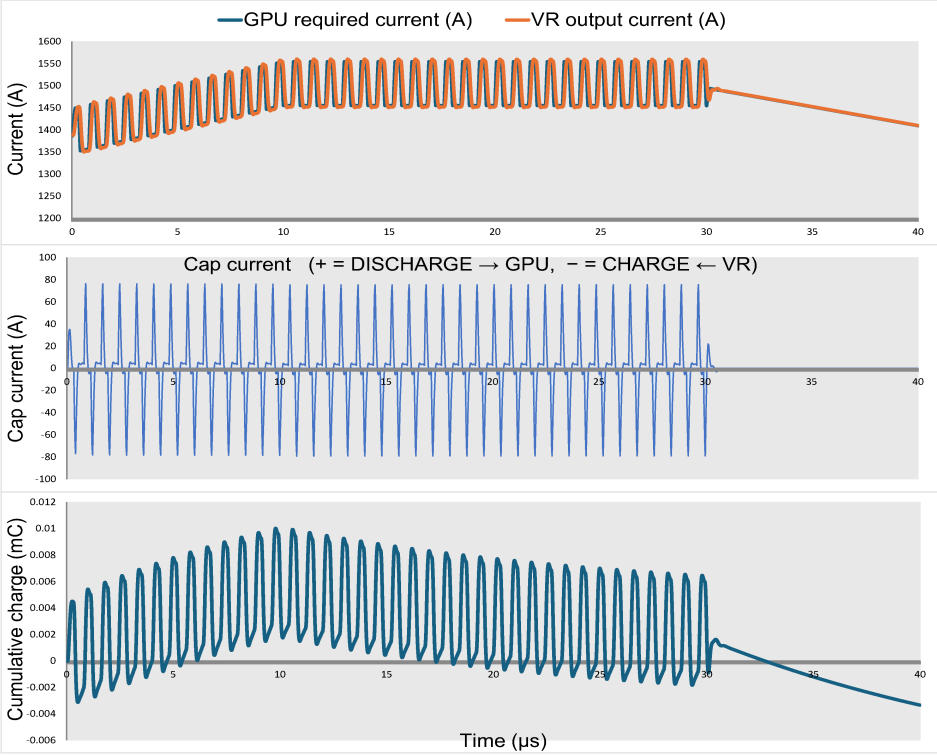
Source: Nomura

Fig. 10: Capacitor charge/discharge and voltage regulator output in response to charge request in Rubin-equivalent model (vertical power delivery)



Source: Nomura

Fig. 11: Capacitor charge/discharge and voltage regulator output in response to charge request in Rubin-equivalent model (IVR)



Source: Nomura

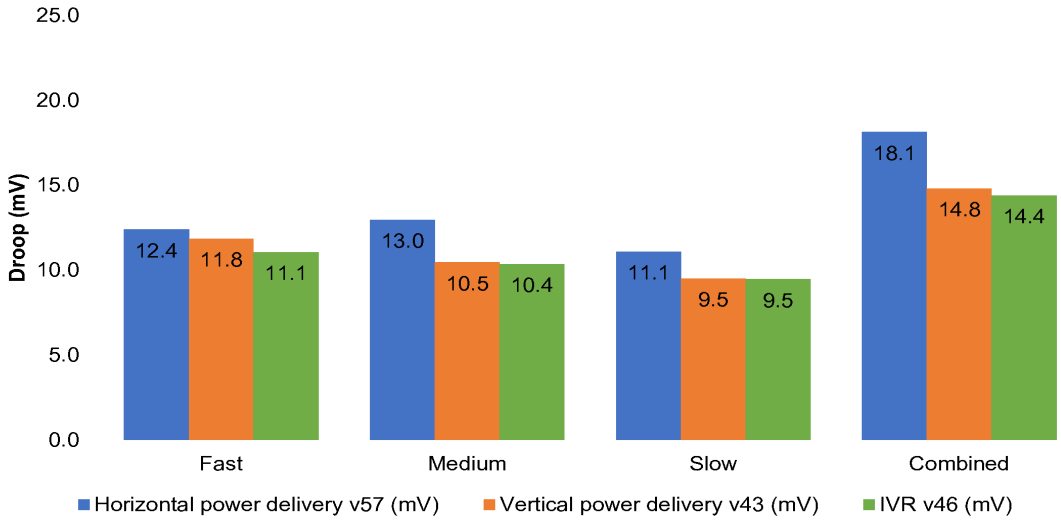
Improvement in responsiveness to changes in voltage regulator load

In lateral power delivery, supply from the voltage regulator cannot keep up immediately following a sharp rise in current demanded by the GPU, and capacitors are used to fill this gap. By contrast, vertical power delivery and IVR offer improved current supply capacity in response to changes in load through a shorter electrical pathway and improvements in voltage regulator responsiveness. Whereas some capacitor discharge is still required in vertical power delivery (Figure 10), there is even less burden on capacitors with the use of IVR (Figure 11), and faster changes in voltage regulator output current in response to changes in current demand.

Changes in role of voltage regulators and capacitors with different supply methods

In this way, changing the power delivery system changes the temporary current and energy requirements of capacitors. This shows that advances in power delivery systems are not just helping to curb GPU voltage droop but are also changing the role of voltage regulators and capacitors themselves. Figure 12 shows a comparison of voltage droop by time window for the different power delivery systems. It shows combined droops of 18.1mV for lateral power delivery but 14.8mV for vertical power delivery and 14.41mV for IVR. Vertical power delivery and IVR have smaller droop than lateral power delivery across all time windows, making them more stable in terms of voltage fluctuations. IVR shows particularly lower droop in the fast window than vertical power delivery.

Fig. 12: Comparison of voltage droop by time window in Rubin-equivalent model

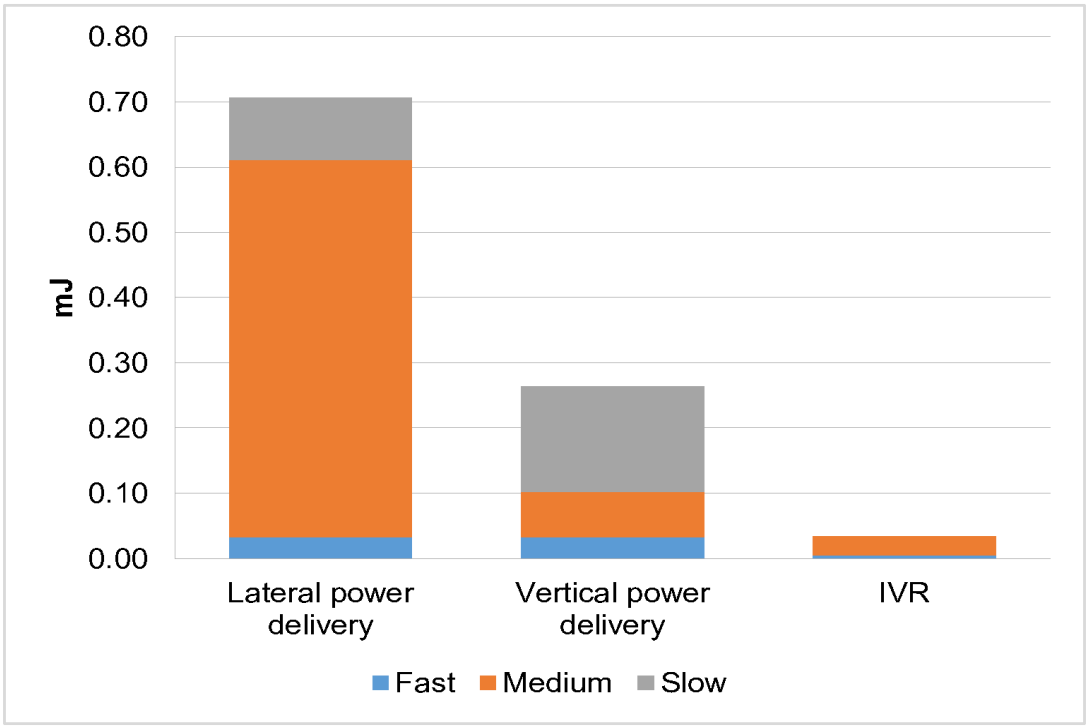


Note: (1) Fast, medium, and slow show the results of simulations of changes in current load for each of the time windows. (2) The combined figure shows the results for the load waveform for 0–10µs and does not necessarily tally with the total of the voltage droop figures by time window. (3) Note that we used a 30% step-load condition for lateral power delivery and a 50% step-load condition for vertical power delivery and IVR.
Source: Nomura

Improvements in medium and slow time windows with vertical power delivery and IVR

Figure 13 shows the energy buffers of the capacitors on the output side of the voltage regulators in each of the power delivery systems by time window. The energy that has to be delivered by capacitors is affected not only by the size of the change in GPU load but also by how fast the voltage regulator can supply the required current. Shortening the electrical pathway or increasing the responsiveness of the voltage regulator to changes in load reduces the amount of time that capacitors are needed to fill the current shortfall gap, thereby reducing the required energy buffer. Our simulations show substantial reductions (improvements) in required energy buffers in the medium and slow time windows with vertical power delivery and IVR than with lateral power delivery. Moreover, IVR offers a greater improvement than vertical power delivery.

Fig. 13: Energy buffer by time window in Rubin-equivalent model

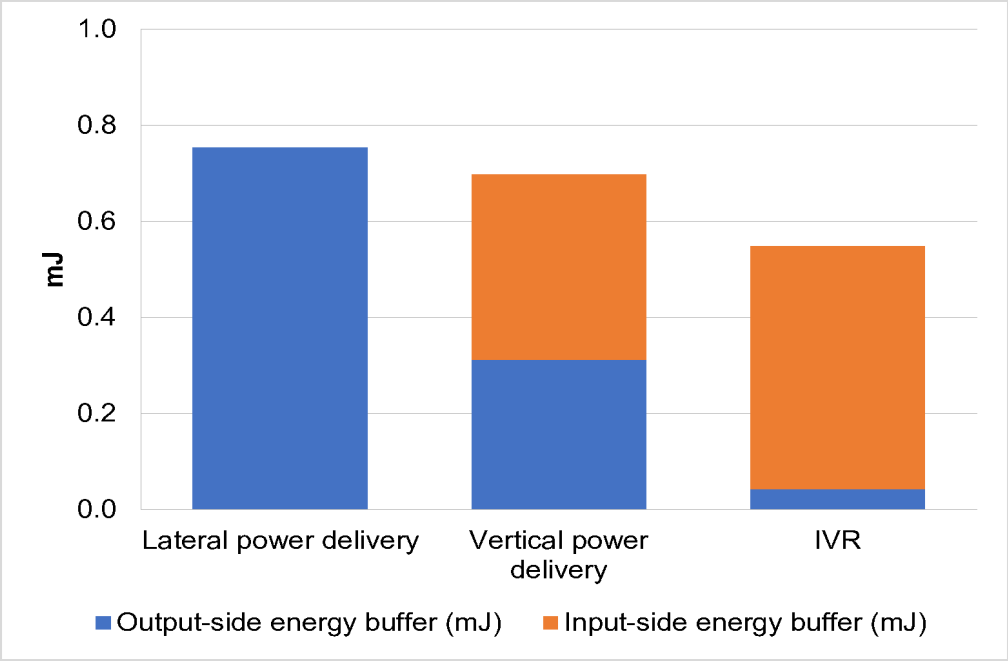


Note: (1) The energy buffer is calculated as the energy that can be delivered from the capacitors on the output side of the voltage regulator within the tolerable voltage ranges for each time window, calculated from their effective capacitance, and does not include the input side of the voltage regulator. (3) Note that we used a 30% step-load condition for lateral power delivery and a 50% step-load condition for vertical power delivery and IVR.
Source: Nomura

Input-side energy buffers crucial for vertical power delivery and IVR

The energy buffers shown here are on the output side of the voltage regulator, and do not include contributions from input-side capacitors, which supply power to the voltage regulator in vertical power delivery and IVR systems. In vertical power delivery and IVR systems, input-side capacitors also support supply of energy to the GPU via the voltage regulator, which means that even if the required energy buffer on the output side declines, capacitor demand for the PDN overall will not necessarily decline by the same degree. Figure 14 shows energy buffer values that include both the voltage regulator input and output sides.

Fig. 14: Energy buffers on the input and output side of the voltage regulator in the Rubin-equivalent model



Note: (1) The energy buffers in Figure 14 are calculated as the energy that can be delivered from the capacitors located on different voltage rails, based on their effective capacitance, and are thus based on different criteria from the energy buffers by time window shown in Figure 13. (2) We assume input-side voltages of 6.75V for vertical power delivery and1.8V for IVR. We use 0.7V for the output side of the voltage regulator for all architectures. (3) Note that we used a 30% step-load condition for lateral power delivery and a 50% step-load condition for vertical power delivery and IVR. We use 0.7V for the output side of the voltage regulator for all architectures.
Source: Nomura

Greater need for higher voltage-rated components on input side than output side

These changes in power delivery design are causing the placement of capacitors used to store energy on the electrical circuit to move from low-voltage rails on the voltage regulator output side to higher voltage rails on the input side. The effective capacitance required will vary depending on the voltage rail used and the tolerable voltage range, even if capacitors are storing the same amount of energy, and generally speaking, the greater the voltage, the smaller the required effective capacitance of a capacitor. Because the prices of capacitors with the same capacitance rises as their voltage resistance increases, the decline in effective capacitance because of the shift to higher voltages does not necessarily imply a decline in value added for capacitors.

Vertical power delivery and IVR systems require less capacitance on output side, new capacitance on input side

When thinking about the changes in capacitor demand depending on power delivery type, we need to consider not only the reductions in capacitance on the output side but also the new capacitance needed on the input side.

Considering physical capacitor positioning and configuration

Figure 15 shows physical capacitor configurations on the output and input sides by power delivery system. It shows that different systems are likely to have very different requirements not only for total capacitance but also for capacitor positioning.

Fig. 15: Comparison of physical capacitor configurations (grouped by mounting location, includes input side)

Placement	Main time window	Lateral power delivery		Vertical power delivery		IVR		*(Reference 1): Vertical power delivery 300kHz voltage regulator bandwidth*		*(Reference 2): Vertical power delivery 200kHz voltage regulator bandwidth*	
		Rated capacitance (mF)	Effective capacitance (mF)	Rated capacitance (mF)	Effective capacitance (mF)	Rated capacitance (mF)	Effective capacitance (mF)	Rated capacitance (mF)	Effective capacitance (mF)	Rated capacitance (mF)	Effective capacitance (mF)
Output side											
In package (MIM, MLCC, silicon cap)	Fast	8.6	3.3	9.1	3.5	2.5	1.8	16.8	6.2	24.6	9.1
MLCCs on PCB backside beneath GPU	Medium	67.3	24.2	8.0	2.9	–	–	*4.0*	*1.4*	*2.0*	*0.7*
Voltage regulator output side (MLCCs, polymer electrolytic capacitors)	Medium-Slow	11.1	4.0	16.6	6.8	–	–	*22.4*	*8.0*	*39.7*	*14.3*
Output side total		**87.1**	**31.5**	**33.6**	**13.1**	**2.5**	**1.8**	*43.1*	*15.7*	*66.4*	*24.1*
Input side											
MLCCs on PCB backside beneath GPU	-	–	–	1.6	0.6	15	5	*1.6*	*0.6*	*1.6*	*0.6*
Main time window	-	–	–	0.2	0.2	6	3	*0.2*	*0.2*	*0.2*	*0.2*
Input side total		–	–	1.8	0.8	20.8	8.1	*1.8*	*0.8*	*1.8*	*0.8*

Note: (1) Rated capacitance is catalog-based capacitance per capacitor multiplied by the number of capacitors. (2) Rated capacity per capacitor: 0603 = 10μF, 1005 = 47μF, 1608 = 100μF, 2012 = 100μF, MIM = Blackwell 100μF/Rubin 300μF, voltage regulator output polymer = 470μF. (3) Effective capacitance is rated capacitance adjusted by derating factors, mF figures shown in the text are effective capacitance unless otherwise stated. The coefficients are 0.36x for MLCCs, 0.8x for voltage regulator output polymer capacitors, and 1.0x for MIM capacitors. (4) Vertical power delivery and IVR systems use a two-stage voltage regulator configuration, and because capacitors are also needed on the input rail (6.75V for vertical power deliver, 1.8V for IVR) of the final-stage voltage regulator, the input side is shown separately. (5) In IVR, the voltage regulator is placed in close proximity to the GPU package, which means there is no independent bank of MLCCs on the PCB backside below the GPU, peripheral MLCCs, or voltage regulator output polymer capacitors (output side). (6) VR output side refers to capacitors connected to the output of the final stage voltage regulator, and their distribution is determined by where the voltage regulator is placed. They are near on the PCB near the GPU in lateral power delivery but on the backside of the PCB below the GPU in vertical power delivery, because the voltage regulator is also placed there, and are mainly used for the medium time window. (7) For reference, we lowered the voltage regulator control bandwidth used in our vertical power delivery from the estimated 400kHz to 300kHz and 200kHz and looked for minimum output-side effective capacitance configurations that would meet the 50% step-load condition. Because using the adopted configuration while lowering the bandwidth causes Z peak to exceed the maximum, we increased capacitance within the package (still 300 capacitors, but 1608 instead of 0603) and on the output side of the voltage regulator and reduced it below the GPU. 300kHz: Z peak of 0.0538mΩ, combined droop of 15.1mV, output-side effective capacitance of 15.7mF. 200kHz: Z peak of 0.0541mΩ, combined droop of 15.3mV, output-side effective capacitance of 24.1mF (roughly 1.8x).

Source: Nomura

Sharp increase in MLCCs below GPU in Rubin-equivalent lateral power delivery

On the output side, using lateral power delivery for the Rubin-equivalent system results in a sharp increase in the capacitance below the GPU. This reflects the need to have capacitance closer to the GPU to make up for the slow responsiveness of the voltage regulator.

Decline in capacitance in vertical power delivery depends on how far voltage regulator bandwidth can be increased

In vertical power supply, the voltage regulator is placed below the GPU, which reduces the effective capacitance of the MLCCs below the GPU from roughly 24mF in lateral power delivery to around 3mF. Meanwhile, capacitance on the output side of the voltage regulator increases from around 4mF to around 7mF because these capacitors, which are located adjacent to the voltage regulator, take over in frequency bands that the voltage regulator cannot respond to. This means that total capacitance on the output side is reduced from roughly 32mF to around 13mF, but the reduction is not uniform. That said, this 13mF figure is for a voltage regulator control bandwidth of 400kHz (estimated). The smaller the bandwidth, the more capacitance is needed as the frequency that the voltage regulator cannot cope with increases. Figure 15 shows capacitance requirements for lower bandwidths for reference. The effective capacitance on the output side is around 16mF at 300kHz and around 24mF at 200kHz, with increases in capacitance in the package and on the output side of the voltage regulator. This shows that the reduction in capacitance in vertical power delivery will depend on the extent to which voltage regulator bandwidth can be increased.

IVR needs less capacitance but involves higher demand in new areas such as package-embedded capacitors

In IVR systems, the output-side capacitors are contained within the package, which means no under-GPU or peripheral capacitors. We have seen moves to use high value-added products such as silicon capacitors for package-embedded applications in IVR, and accordingly look to an increase in value-added unrelated to capacitance requirements.

Higher capacitance requirements on input-side voltage rail than on output side makes it difficult to carry out simple comparison of parts

Moreover, having fewer capacitors on the output side does not mean a decline for the PDN overall. Vertical power delivery and IVR systems require new capacitors on the input side of the voltage regulator, and these are used to supply some of the energy needed during load fluctuations. Energy buffers are dictated not only by effective capacitance but also by the voltage rails being used and the tolerable voltage range, and because of this, a simple sum of the effective capacitance on the output and input sides will not provide

any insight into the differences in capacitor requirements for the different power delivery systems.

Further developments in power delivery systems likely to change component types and mounting locations

As power delivery systems change, we are likely to see changes in the distribution of capacitors between the output and input sides and in the types of components needed and where they are located, rather than just a simple decline in capacitor demand.

3. Considerations and investment recommendations: Advances in PDNs and impact on passive parts industry

(1) Thoughts on simulation models

Increasing performance of GPUs and constraints on lateral power delivery design

As AI processor performance increases, their PDNs require not only the supply of large amounts of current in a stable fashion but also the ability to cope with sudden changes in load. As power consumption increases, the same step-load percentage will cause a bigger variation in current, which means a lower target impedance is needed to keep voltage within its tolerable range.

Review of simulation results

Our simulations showed that the use of lateral power delivery for the Blackwell-equivalent processor met the 50% step-load condition but using lateral power delivery for the Rubin-equivalent processor resulted in impedance exceeding its upper bound under the same condition. Design criteria were met with the Rubin-equivalent processor by easing the step-load condition to 30%, but this reduced leeway versus the tolerable maximum.

Difficult to cope with rising GPU power consumption with lateral power delivery

These results suggest that as processor power consumption increases, it will get harder to cope with sharp fluctuations in load with conventional lateral power delivery. Increasing capacitor count on the PCB side has little impact, with the only effective measure being increasing capacitance within the package close to the GPU, but there is limited mounting space within the package. Moreover, even if voltage regulator responsiveness is improved, performance will still be affected by the resistance of the supply pathways to the GPU and loop inductance. Wiring resistance can have an impact on power losses as well as voltage stability. Accordingly, we think future PDNs will require increased performance in the capacitors and voltage regulators themselves, and integrated design, including the power delivery system, will also be crucial.

Shift to vertical power delivery and IVR systems and role of power supply components

Vertical power delivery and IVR are technologies that shorten the power supply pathway by bringing the voltage regulator closer to the GPU than in lateral power delivery systems. In our Rubin-equivalent model, impedance exceeded its tolerable upper bound by only around 2% in vertical power delivery at a step-load condition of 50%, and design criteria were met with IVR.

Brining voltage regulator closer to the processor

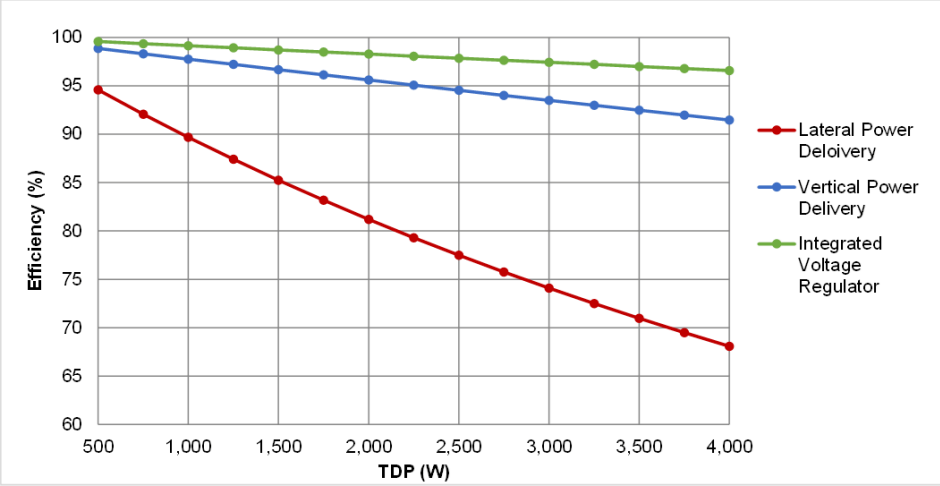
Shortening the power supply pathway makes it easy to deliver current from the voltage regulator to the GPU quickly, and reduces the need to use output-side capacitors to make up for current shortfalls when the load changes. In other words, we think PDN development is shifting from increasing the number of capacitors to make up for the slow responsiveness of voltage regulators towards improving current supply itself by positioning the voltage regulator closer to the processor under load.

Shortening power delivery pathway also reduces power losses

Shorter power delivery pathways also help to improve power efficiency as well as responsiveness. The wiring from the voltage regulator output to the GPU has resistance, and losses increase in proportion to the square of the current. In our model, power consumption approaches 2,250W, which means power distribution losses from the voltage regulator output to the GPU of around 260W with lateral power delivery, around

50W with vertical power delivery, and around 20W with IVR (Figure 16). Our calculations show that roughly 20% of the power output of the voltage regulator is lost in the wiring in lateral power delivery. Increasing power consumption to 4,000W would increase losses in lateral power delivery to around 820W. The more GPU power consumption increases, the more effective bringing the voltage regulator closer to the GPU becomes.

Fig. 16: Comparison of power delivery efficiency (from voltage regulator output to GPU, %)



Note: (1) Loss ratio = wiring losses ÷ power reaching the die. Losses are proportional to the square of TDP (because current is proportional to TDP and losses are R × I²). Accordingly, the loss ratio increases more or less proportionately with TDP. (2) Current is calculated by multiplying the Vcore rail current (TDP × 0.65 ÷ 0.7V) by a factor ranging from the idle rate of 0.65 through to peak of around 0.73. A TDP of 2,300W gives idle of 1,388A and peak of 1,554A. (3) Pathway R: lateral power delivery 110μΩ, vertical power delivery 10μΩ, IVR 2μΩ. Packaging to die is common across all three systems (10μΩ × 2, parallel). VR phase DCR: lateral/vertical 0.4mΩ ÷ 40 phases, IVR 0.1mΩ ÷ 40 phases. All figures are model assumptions. (4) Models: Rubin lateral power delivery v57, vertical power delivery v43, IVR v46 (26 Sep 2026). Time periods for load waveform set at 35 μs/load clearance 25 μs in all three systems. Yellow lines indicate key points (1,000W, 2,250W, 4,000W).
Source: Nomura

Making components smaller, more efficient, and heat-resistant is key

However, bringing the voltage regulator closer to the GPU reduces the space where large currents are handled, which means power converter circuits have to be smaller, more efficient, and heat-resistant. Going forward, we think the challenge will be achieving the electrical advantages of shorter power supply pathways and high-density voltage regulator mounting.

Increasing importance of inductors in reducing size and increasing performance of voltage regulators

We think inductors and other magnetic components will be increasingly important in making voltage regulators smaller while also increasing their tolerance to large currents and high-speed transient response.

Making inductors smaller and more performant crucial to making voltage regulators smaller

While reducing inductance results in faster current rise time, it also causes increases in ripple current and losses. Other problems that need addressing include not only dealing with magnetic saturation as the current increases but also curbing winding losses, core losses, and heat generation in a restricted mounting space. The magnetic coupling technology used in the trans-inductor voltage regulators (TVLRs) we assume in all our Rubin-equivalent models is one solution for improving voltage regulator transient response.

Need for small/low profile, low-loss, high heat-dissipation products

Accordingly, when it comes to voltage regulators that use inductors, magnetic components that combine high current handling capabilities, low losses, low profiles, and thermal performance are a key element in increasing mounting density in the PDN. In our view, advances in power delivery systems will bring about changes not only for capacitors put also in the performance requirements for the inductors used in voltage regulators.

Quantitative and qualitative changes in capacitor demand

These changes in power delivery system are also changing the role that capacitors play. Lateral power delivery systems require substantial capacitance from output-side capacitors below the GPU or in peripheral locations on the PCB to deal with the slow responsiveness of the voltage regulator. By contrast, vertical power delivery and IVR systems have shorter power supply pathways on the output side, which changes the capacitance needed and mounting locations. Vertical power delivery moves the capacitors connected to the output side of the voltage regulator to below the GPU, in tandem with the voltage regulator. Understanding capacitor demand for the different power delivery systems will need to take account not just of total capacitance and total capacitor count but also looking at demand on the input and output sides and by mounting location.

We forecast growth in demand for compact, high-capacitance MLCCs for lateral power delivery, package-embedded capacitors for vertical power delivery and IVR

In terms of component characteristics, we think compact, high-capacitance MLCCs with low ESL are key for lateral power delivery as it requires high-density mounting of large amounts of capacitance directly below the GPU. By contrast, vertical power delivery and IVR systems need components with the right capacitance and voltage ratings for the input-side high-voltage rails and low-inductance capacitors that can be placed inside or in proximity to the package. We also think it will be important to distinguish products such as MIM and silicon capacitors in terms matching the mounting location.

Component heat resistance and long-term reliability likely to be crucial too

Moreover, selecting components for configurations that place the voltage regulator close to the GPU require consideration not only of electrical characteristics but also heat resistance and long-term reliability. Capacitors will have to maintain the necessary effective capacitance and ESR characteristics at expected operating temperatures (105° C-rated at present, 125°C-rated in future), and also cope with the heat associated with ripple current too. The actual temperature of the components depends on the heat generated by the GPU and voltage regulator, the cooling system, and mounting location, which means that evaluating thermal requirements will have to be based on the thermal design of the system.

Advances in power supply architecture design are changing component demand

This shows that capacitor demand will not necessarily increase uniformly in line with GPU power consumption. Changes to PDN architectures are changing not only the required effective capacitance but also requirements in terms of the types of products, rated voltage, mounting location, and heat resistance. When considering the impact on the capacitor market, we will need not only to factor in rises or declines in the number of parts used but also changes in the demand mix.

(2) Positioning of simulation results

Simulations of virtual processors and not specific products

The simulations in this report are of virtual processors with the same electrical characteristics as Blackwell and Rubin processors and are not meant to reproduce the actual internal circuitry or components used in Nvidia products.

Differences in capacitor and component count not dictated by differences in power delivery alone

Moreover, our simulations used different load criteria for the Rubin-equivalent processor, with a 30% step-load condition for lateral power delivery and a 50% condition for vertical power delivery and IVR. Our model also gave a conditional result for vertical power delivery, in that impedance was slightly higher than its acceptable upper bound. Moreover, the results for our vertical power delivery model assume a control bandwidth of 400kHz (estimated), and a bandwidth of 300kHz would require effective capacitance on the output side of around 16mF, or around 24mF at 200kHz (Figure 15). Accordingly, the differences in capacitance and capacitor count between the different models is not simply the result of changing the power delivery system.

We did not carry out thermal design, will have to look at the details going forward

In addition, the analysis presented in this report was primarily on the electrical performance and physical capacitor configurations, and we did not make any quantitative evaluation of component temperatures or lifespans. We will need to scrutinize the details about thermal design and mounting constraints in future. Our estimates for power

distribution losses only looked at the losses from resistance between voltage regulator output and GPU, and did not include conversion losses in the voltage regulator itself or losses from the wiring on the input side of the voltage regulator. Current also flows through the rails on the input side in vertical power delivery (at 6.75V) and IVR (at 1.8V), and the actual differences may be smaller than our calculations. Our 110μΩ figure for wiring resistance in lateral power delivery is an assumption.

Analysis provided as one possible scenario

We present this analysis as one scenario for thinking about the constraints placed on the PDN from increasing GPU power consumption and the changes in the roles of capacitors and voltage regulators in new power delivery systems.

(3) Stock recommendations

Murata Manufacturing: Strengths in overall capacitor capabilities and module development

Murata Manufacturing's strength lies in its comprehensive capabilities in developing multiple types of MLCC targeting a wide range of application markets as well as its broad product and technology base, spanning silicon capacitors, inductors, and technologies to embed passive parts into substrates.

This includes its Integrated Package Solution (iPaS), where capacitors and inductors are embedded into the substrate, offering a means of reducing space requirements and improving electrical characteristics. Its capacitor-embedded substrates shorten electrical pathways and reduce inductance by incorporating high-capacitance capacitors and current-carrying through-holes directly into the substrate. Its inductor-embedded substrates are designed to reduce the profile of power supply modules and increase mounting density by embedding planar coil arrays into the substrate. The company has so far developed these as separate products, but it is aiming to develop substrates embedded with both capacitors and inductors in the future.

The company has also been developing voltage regulator modules for vertical power delivery, which feature iPaS capacitor-embedded substrates, and we expect these to go into mass production from 2027 onwards for use as output-side capacitors. The models in this report require effective capacitance of around 7mF on the output side of the voltage regulator in vertical power delivery, and we view iPaS capacitor-embedded substrates as a technology to replace these capacitors with embedded capacitors. While increased use of iPaS will reduce demand for surface mounted MLCCs in volume terms, Murata Manufacturing will likely be focusing on value-added per unit through the supply of these voltage regulator modules.

In configurations that place the voltage regulator close to the GPU, it is not simply a question of having substantial capacitance, but the power supply circuitry has to be squeezed into a limited space in order to achieve shorter electrical pathways. Having the technologies to embed both capacitors and inductors into substrates is a strength not just for improving the performance of standalone components but also in terms of design, including for power supply modules and electrical pathways.

Meanwhile, thin-film, low-inductance silicon capacitors are crucial in configurations such as IVR that concentrate capacitors inside or close to the package. Murata Manufacturing offers high-density silicon capacitors that use semiconductor manufacturing processes, and are notable for their capacitance stability versus temperature and voltage, their low profile, and fine-grained mounting compatibility. These products are a good match for dealing with rapid load fluctuations in limited spaces close to the GPU. Looking ahead, we see potential for iPaS substrates embedded with both capacitors and inductors to find use as package substrates for IVR.

Murata Manufacturing has technologies for all areas of PDNs, including compact, large-capacitance MLCCs that are key in lateral power delivery, iPaS for vertical power delivery, silicon capacitors that are playing an increasingly important role in IVR, and inductors that help make voltage regulators smaller. We think having a broad range of products and technologies that can cope with changes in the parts and mounting technologies needed, however power delivery systems develop, is a major strength for the company.

TDK is strong in thin-film inductors and high-voltage parts

TDK excels in high-voltage, high-temperature, high-reliability passive parts for industrial machinery and automotive applications. While it is more competitive in high-voltage passive parts for the power distribution side of data centers (MLCCs, aluminum electrolytic capacitors, film capacitors, varistors etc), we expect its products to find use in PDNs going forward too.

IVR uses technologies to increase the current response to changes in load through the magnetic binding of inductors of multiple phases, and requires these inductors to be mounted in the package substrate. TDK has developed thin-film inductors using the manufacturing processes it has built up in HDD magnetic heads to create products that have lower losses while being small and low profile. We expect them to find use in IVR systems from 2027 onwards. IVR systems have to handle large currents in a limited mounting space and have high-speed transient response, and TDK's thin-film inductors are ideal for these thanks to their low profile, low losses, and low direct current resistance (DCR).

We think thin-film inductors will find use in voltage regulator modules for vertical power delivery and not just in IVR. Voltage regulators in vertical power delivery have greater current per phase than IVR systems, which means the inductors need to be resistant to magnetic saturation even at high currents. TDK's thin-film inductors use its proprietary magnetic materials with high saturation flux density, and are suited to these kinds of high currents. In addition, their low losses at high frequencies makes it easier to increase voltage regulator switching frequency, helping to improve voltage regulator responsiveness in vertical power delivery. The simulations in this report show that lowering the control frequency of the voltage regulator in vertical power delivery increases the effective capacitance needed on the output side from around 13mF to around 24mF. The high-frequency characteristics of inductors thus also effect required capacitance via voltage regulator responsiveness.

TDK has also been working to develop compact, high-capacitance MLCCs with good capacitance stability versus temperature and voltage using the foundational technologies it has built up in automotive products. Vertical power delivery and IVR systems place the voltage regulator close to the GPU, which increases the exposure of components to high temperatures, and we accordingly expect growing demand for products with high reliability even under high temperatures. TDK signed a memorandum of understanding with Taiyo Yuden [6976] about joint development of MLCCs and inductors at the end of September 2026, and we think this will be a positive for the development of high temperature-rated MLCCs at both companies. TDK is strong in high-voltage, high-reliability products, while Taiyo Yuden's strengths lie in its high density stacking technologies that can create over 1,000 layers and its technologies for mass production of fine-grained barium titanate using solid-phase synthesis. We think combining the two companies' technologies will enable stable mass production of compact, high-capacitance products with high temperature ratings at an early juncture.

We think TDK will see growth not only in high-voltage passive parts for data centers but also for new products such as thin-film inductors developed for next-generation PDNs. Successful collaboration with Taiyo Yuden or with Nippon Chemical Industrial [4092], with which TDK has set up a JV, could increase its competitiveness in high-temperature rated MLCCs for next-generation PDNs.

(4) Others

Initiatives at Taiyo Yuden and Kyocera

Taiyo Yuden has strengths in reducing the size of its MCOIL stacked metal inductors, and we expect them to be used in power supply modules in vertical power delivery systems. Its metal inductors feature a material technology in which a nanoscale, highly crystaline oxide layer is grown on iron-based magnetic particles, thereby ensuring electrical insulation while also achieving high-density magnetic bonding. This material has high magnetic permeability and is highly competitive in the ultra-compact domain. Kyocera [6971] has technologies for fixing terminals on the top and bottom sides of MLCCs using conductive vias, and can manufacture MLCCs suited to being embedded in packages and circuit board modules that include MLCCs. It also has industry-leading capabilities in compact, high-capacitance MLCCs. We forecast growth in sales for data center applications.

Fig. 17: Appendix A: Design criteria and step-load conditions

Criteria used to gauge PDN success/failure and step-load conditions used in simulations

Item	Blackwell-equivalent	Rubin-equivalent (common to Lateral, VPD and IVR)	Remarks
Design criteria (policy A of 2026-09-26)			
Target impedance Z_target	(Allowed droop - static IR drop) / (step fraction x peak current)	Same as left	Maximum impedance that keeps the voltage deviation within the allowance for the load step
Combined allowed droop	37.5 mV (5% of VDD)	35.0 mV (5% of VDD)	Baseline is 5%. 4% is also evaluated when margin allows (record only)
Fast allowed droop	14.8 mV (2% - 0.2 mV guard)	13.8 mV (2% - 0.2 mV guard)	Relaxed to 2.5%, then 3% if not met (all models pass at 2% here)
Z-peak limit (1 kHz - 1 MHz)	1.5×Z_target = 0.178 mΩ	1.5×Z_target	Conditional pass: within +3% of the limit
Control gain	Kp = 1/Z_target, Ki = Kp×6×10⁴	Same as left	
Load conditions (assumptions; not specifications of actual NVIDIA products)			
Power / core voltage	1000 W / 0.75 V	2300 W / 0.70 V	Rubin-equivalent power is an estimate from public information
Core rail share	0.60	0.65	
Peak current	588.4 A	1,554.4 A	
Static IR drop	2.6 mV	6.94 mV	
Load step fraction (adopted)	50%	Lateral 30% / VPD 50% / IVR 50%	Lateral at 50% and 35% fails at the physical limit (Figures 6 and 7)
Load step current	294.2 A	Lateral 466.3 A (30%) / VPD and IVR 777.2 A (50%)	
Load waveform rise	10 ns	75 ns	Edge time
Load period / duty	1.0 µs / 0.35	0.8 µs / 0.40	Idle fraction 0.65
Load excursion by time window (Fast / Medium / Slow)	7.5% / 5% / 5%	Same as left	Medium rise 1 µs, Slow 10 µs
Clock ramping	Enabled (rate parameter Medium 0.01/µs, Slow 0.0025/µs)	Enabled (Medium 0.005/µs, Slow 0.002/µs)	Downward rate is 2x
Time windows evaluated	Fast (up to 150 ns) / Medium (up to 1 µs) / Slow (up to 10 µs) / Combined (0-10 µs actual load)	Same as left	Worst value over the three GPU-under L corners is adopted

Source: Nomura

Fig. 18: Appendix B: Conditions by model (voltage regulator, power supply pathway, control)

Item	Blackwell-equivalent	Rubin Lateral	Rubin VPD (vertical power delivery)	Rubin IVR (integrated VR)
Delivery path				
VR-to-package path L / R	20 pH / 110 µΩ	20 pH / 110 µΩ	10 pH / 10 µΩ	2 pH / 2 µΩ
DSC access L / R	0.67 pH / 5 µΩ	0.67 pH / 5 µΩ	0.67 pH / 5 µΩ	0.67 pH / 1.05 µΩ
LSC access L / R	3.20 pH / 5 µΩ	3.20 pH / 5 µΩ	3.20 pH / 5 µΩ	3.20 pH / 5 µΩ
GPU-under access L (3 corners)	6.40 / 10.76 / 32.60 pH (as is)	3.20 / 5.38 / 16.30 pH (×0.5)	3.20 / 5.38 / 16.30 pH (×0.5)	None (no GPU-under bank on the output side)
Die-side local L / R / Cdie	4.0 pH / 10 µΩ / 40 µF	2.46 pH / 10 µΩ / 80 µF	2.46 pH / 10 µΩ / 80 µF	2.46 pH / 10 µΩ / 80 µF
VR				
VR control bandwidth	100 kHz	150 kHz	400 kHz (inferred)	3 MHz
Kp / Ki	8,430 A/V / Kp×6e4	16,620 A/V / Kp×6e4	27,700 A/V / Kp×6e4	27,700 A/V / Kp×6e4
Phases / L per phase / R per phase	30 phases / 100 nH / 0.4 mΩ	40 phases / 100 nH / 0.4 mΩ	40 phases / 100 nH / 0.4 mΩ	40 phases / 10 nH / 0.1 mΩ
TLVR magnetic coupling	Disabled	Enabled (k = 0.95, turns ratio 1, compensation L 20 nH)	Enabled (same as left)	Enabled (same as left)
VR input voltage	12 V (ideal source)	12 V (ideal source)	6.75 V (with input-side capacitors)	1.8 V (with input-side capacitors)
Current slew-rate cap / maximum current	600 A/µs / 1,500 A	1,000 A/µs / 2,800 A	1,000 A/µs / 2,800 A	4,000 A/µs / 2,800 A
Inner control time constant	0.1 µs	0.1 µs	0.1 µs	0.02 µs
Boost (transient boost control)	OFF	OFF	OFF	OFF
Simulation time	60 µs	40 µs	35 µs	40 µs
Judgement				
Judgement of the adopted configuration	PASS	PASS (30%)	CONDITIONAL (+2.0%)	PASS (input droop 33.9 mV <= 35 mV)

Note: (1) Blackwell uses original physical conditions (100kHz bandwidth, no change to L below GPU). We assume a realistic scenario for Rubin lateral and vertical power delivery (L below GPU × 0.5, higher bandwidth). (2) Bandwidth of 400kHz for vertical power delivery is an estimate and not a disclosed figure. 3MHz for IVR is lower than the disclosed figure of over 10MHz. (3) Input sides for vertical power delivery and IVR are divided into RLC circuits according to voltage regulator input voltage (tolerable fluctuations of 75mV for vertical power delivery, 35mV for IVR). (4) Averaged model (40-phase decomposition for IVR has been shown to be the same as the aggregated model).
Source: Nomura

Appendix A-1

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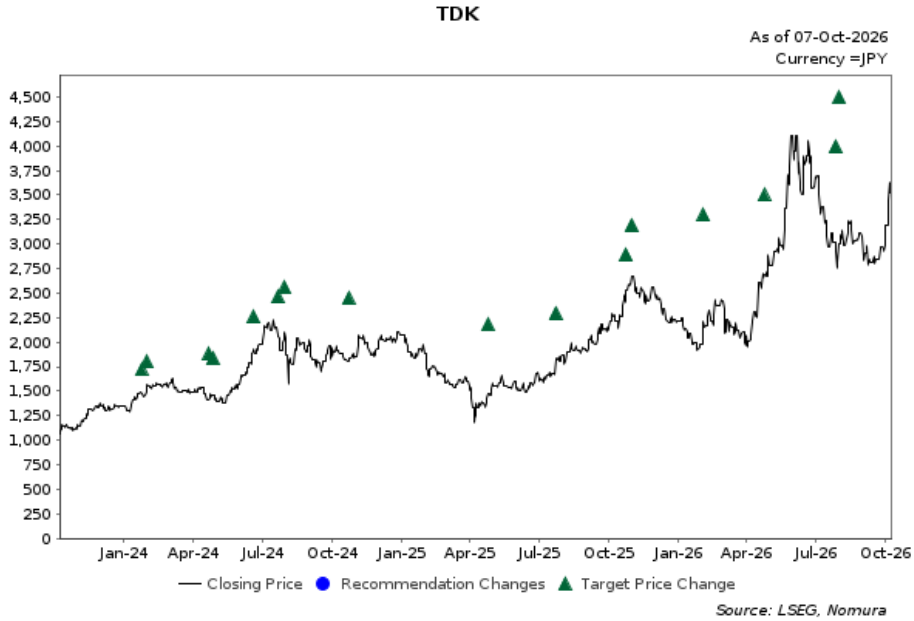
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Issuer	Ticker	Price	Price date	Stock rating	Sector rating	Disclosures
TDK	6762 JP	JPY 3,530	07-Oct-2026	Buy	N/A	A4,A5,A6,A7,A11,A16
Murata Manufacturing	6981 JP	JPY 8,683	07-Oct-2026	Buy	N/A	A4,A5,A6,A11

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TDK (6762 JP) **JPY 3,530 (07-Oct-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)



Date	Rating	Target price	Closing price
01-Aug-26		4,500	3,008
27-Jul-26		4,000	3,012
24-Apr-26		3,500	2,689.5
03-Feb-26		3,300	2,212.5
31-Oct-25		3,200	2,673.0
24-Oct-25		2,900	2,528.5
23-Jul-25		2,300	1,815.0
25-Apr-25		2,180	1,468.0
23-Oct-24		2,450	1,806.5
31-Jul-24		2,560	2,107.0
22-Jul-24		2,460	2,079.0
20-Jun-24		2,260	1,933.2
27-Apr-24		1,840	1,462.4
22-Apr-24		1,880	1,418.4
31-Jan-24		1,800	1,488.4
24-Jan-24		1,720	1,479.0

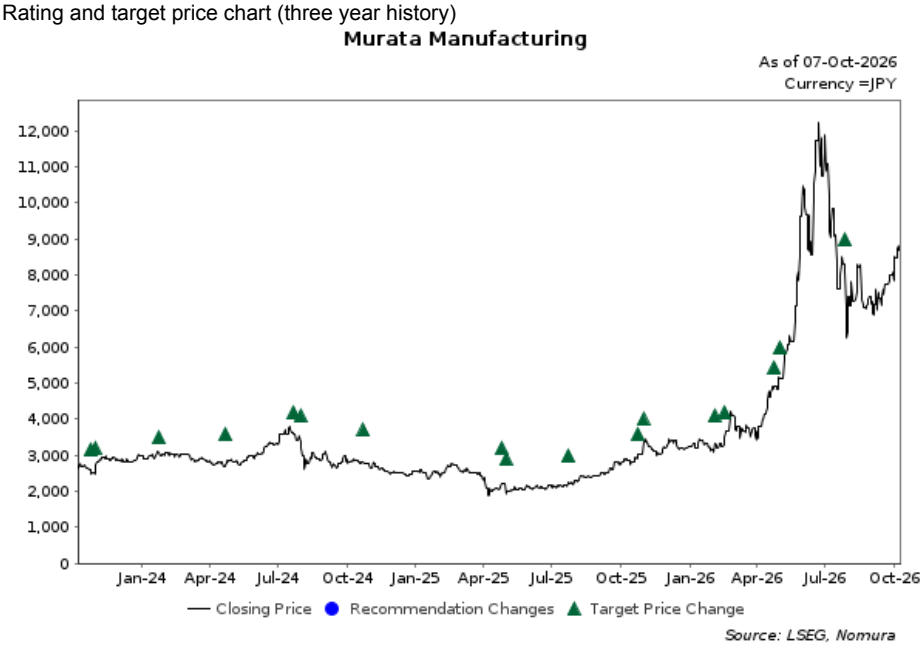
For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology We use DCF analysis based on earnings forecasts for the next three fiscal years to calculate our target price of ¥4,500. We assume a cost of equity capital of 5.0% and terminal growth of 0%. We use corporate value of ¥200.0bn (27/3, after-tax present value of ¥115.0bn included in corporate value) for its 30% stake in a cell joint venture that manufactures medium-capacity batteries.
Risks that may impede the achievement of the target price Factors that could keep the share price from approaching our target price include a stalling in the economy, inventory adjustments at customers, and rapid strengthening of the yen versus the US dollar. Further delays in structural reforms for businesses suffering from low earnings, such as magnets, could undermine confidence in management and result in higher capital costs. Li-ion batteries make heavy use of cobalt, and a rise in cobalt

prices could cause margins to fall temporarily, but the company has signed agreements with customers that revise prices on a quarterly basis to reflect metal prices, and we thus see negligible impact.

Murata Manufacturing (6981 JP) **JPY 8,683 (07-Oct-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)



Date	Rating	Target price	Closing price
27-Jul-26		9,000	8,102
01-May-26		6,000	5,138
24-Apr-26		5,450	4,936
17-Feb-26		4,200	3,509
03-Feb-26		4,100	3,318
31-Oct-25		4,000	3,392
24-Oct-25		3,600	3,018
23-Jul-25		3,000	2,232.5
01-May-25		2,900	1,930.5
25-Apr-25		3,200	2,220.0
23-Oct-24		3,700	2,793.5
31-Jul-24		4,100	3,351
22-Jul-24		4,200	3,581
22-Apr-24		3,600	2,745.5
24-Jan-24		3,500	3,091
31-Oct-23		3,200	2,477.5
25-Oct-23		3,170	2,599.5

For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology We use DCF analysis based on earnings forecasts for the next three fiscal years to calculate our target price of ¥9,000. We assume a cost of equity capital of 4.0% and terminal growth of 0%.
Risks that may impede the achievement of the target price Factors that could cause the share price to come in well below our target price include Among risks that could cause the share price to fall substantially short of our target price, a further macroeconomic slowdown in more economically developed countries could trigger inventory downsizing for MLCCs and other commodity parts. Chinese companies have started to enter the low-end RF communications parts market. If industry realignment were to take place as a result of companies in more economically developed countries making moves to retain customers in technology and high-end markets, and Murata Manufacturing were not part of this, we think it could be exposed to even fiercer competition than it is now.

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