Asia Semiconductor Insight

AI put to the test: the new era of chip testing

Equities

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Time to revisit semiconductor testing as content growth accelerates

Our core thesis is that AI-driven chip complexity is drastically increasing testing content across wafer, package, and system levels, creating a multi-year growth opportunity that the market has yet to fully price in. Testing companies in Taiwan have underperformed TAIEX in the past three months (indexing at -9% vs TAIEX +7%), yet to recover from the July market deleveraging. Investor hesitation currently stems from 1) fear of test content growth expectations already priced-in, 2) lingering concerns over shorter test times, and 3) near-term capacity constraints among major suppliers of probe cards, load boards, socket pins, testers, and handlers, caused by heightened testing demand. Ultimately, these concerns overshadow the structural increase in test insertions required by AI accelerators, chiplets, and advanced packaging. As advanced packaging scales, testing intensity must rise in tandem, driving growth through higher content per device rather than semiconductor unit growth alone.

Expanding testing opportunities with shift-left for CP and increasing FT content

Chip probing (CP) supply chain should be the key beneficiary of the industry's shift-left testing trend, as more test insertions move to the wafer level before packaging, in addition to longer CP time. We believe investors underestimate this trend, which should accelerate with broader adoption of 2.5D/3D packaging, chiplets and larger AI packages, driving demand for high pin count probe cards, probers, and thermal-control equipment. We expect strong growth for **Hermes Testing (HTSI)** as thermal-management requirements rise with increasing chip power and complexity, with prober thermal-control module shipments reaching 3,000/4,100 units in 2027E/28E, up from 1,200 in 2026E. We forecast **Chunghwa Precision Test (CHPT)**'s sales to exceed consensus by 7%/15% in 2027E/28E, supported by structural AI/HPC testing demand and rising value-added content. Importantly, shift-left testing does not diminish the role of final test (FT) and mission-mode testing. Test content and test time should continue to increase as validation becomes increasingly critical for complex, large-form-factor AI accelerators. We expect larger package sizes and rising system-level testing requirements to drive demand for **WinWay**'s high-pin-count sockets, supporting 74%/71% YoY sales growth in 2027E/28E.

Future of testing: co-packaged optics (CPO) will be a major opportunity

CPO testing represents a significant new market opportunity, though we expect the ecosystem to remain fragmented rather than consolidating around a single winner. As AI scaling shifts the industry bottleneck from memory to interconnect, CPO adoption is becoming increasingly important, creating new testing challenges that will require collaboration across equipment, optics, and test solution providers. Leveraging ficonTEC's optical alignment expertise and **HTSI**'s probe, testing, and manufacturing capabilities, we estimate the HTSI will deliver 40 units of insertion 2 equipment and 70 units of insertion 3 testing equipment in 2027, with further upside in 2028 as CPO deployment expands from scale-out towards scale-up.

Initiate Hermes Testing, Chunghwa Precision Test, WinWay with Buy ratings

We initiate coverage on semiconductor testing solution provider **Hermes Testing with a Buy rating, NT$8,880 price target** based on 31x 2028E PE, for thermal control/CPO with the most attractive risk/reward in our testing coverage; test interface PCB supplier **CHPT with a Buy rating, NT$5,000 price target** based on 31x avg 2027-28E PE, for CPU/TPU programs and test board content gain; and semiconductor test socket leader **WinWay with a Buy rating, NT$8,900 price target** based on 30x avg 2027-28E PE, for socket content growth and margin recovery. Among our testing coverage, we also like Hon Precision and Chroma ATE.

This report has been prepared by UBS Securities Pte. Ltd., Taipei Branch. **ANALYST CERTIFICATION AND REQUIRED DISCLOSURES, INCLUDING INFORMATION ON THE QUANTITATIVE RESEARCH REVIEW PUBLISHED BY UBS, BEGIN ON PAGE 22.**

UBS Research THESIS MAP	MOST FAVORED	LEAST FAVORED
	HTSI, CHPT, WinWay, Hon Precision, Chroma ATE	N/A

PIVOTAL QUESTIONS

Q: Is chip probing becoming increasingly important in the testing supply chain?

Yes. As package costs rise, foundries must improve known-good-die (KGD) screening before packaging, increasing demand for wafer-level testing. This should drive demand for probe cards, probers and advanced thermal control solutions capable of managing higher power consumption, wafer warpage and tighter test tolerances. We forecast HTSI/CHPT/WinWay' probe card business to see a 31%/35%/33% sales CAGR for 2026-2031E, as they are positioned to grow strongly given their smaller scale and robust growth drivers from shift left, CPU, AI accelerators. We forecast HTSI to ship 1,200/3,000/4,100 thermal control modules in 2026E/27E/28E, as advanced wafer-level test for AI accelerators will require thermal control solutions in order to prevent probe card needle burnt.

Q: Will FT and SLT content continue to grow in the coming years?

Yes. Despite concerns that final-test (FT) time could flatten or decline with Nvidia's Rubin GPUs, we expect overall FT content to continue growing as advanced packaging complexity and chip sizes increase. We also expect broader adoption of system-level testing (SLT)/mission-mode testing, as AI accelerators require increasingly stringent validation to ensure optimal system and rack-level performance. We forecast WinWay's socket business to see a 33% sales CAGR for 2026-2031E.

Q: Will CPO testing be a revenue generator in 2027-28 to supply chain players?

Yes. Testing remains a key bottleneck, creating a new equipment opportunity beginning in 2027E. We expect initial CPO volumes in 2027, followed by broader adoption in 2028. Testing remains one of the key bottlenecks to commercialization, driving demand for new equipment and test solutions. We believe early leaders such as ficonTEC (partnership with HTSI) are well positioned to benefit from the initial ramp, alongside suppliers including Chroma ATE and Hon Precision.

WHAT´S PRICED IN?

1) We believe upside from agentic AI CPU demand is not reflected in CHPT and WinWay shares. We estimate CPU-related demand could contribute 20-30% of 2027E sales for CHPT and WinWay, respectively, with further upside in 2028E. **2)** We believe market expectations for 2027 CPO testing equipment shipments remain conservative, particularly for insertion 2 equipment. Based on our industry analysis, we estimate HTSI will deliver 40 insertion 2 and 70 insertion 3 systems in 2027E, this should be higher than the market's expectation of no insertion 2 and limited insertion 3 shipment due to engineering bottleneck. We also see further upside in 2028E as CPO adoption expands.

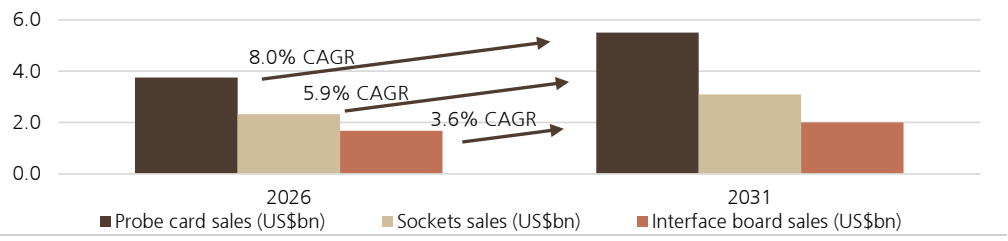
UBSVIEW

Testing is becoming one of the largest incremental beneficiaries of AI-driven semiconductor complexity. As more test insertions are required across wafer, package and system levels, testing content per device should increase materially, expanding the industry's addressable market and supporting multi-year growth across the supply chain.

EVIDENCE

TSMC and OSATs have been expanding their CoWoS capacities aggressively, from 40kwpm in 2024 to around 90 kwpm in 2025, and tracking to expand CoWoS capacity toward 160kwpm in 2026E. TSMC also ramped up expanding N3/N2 capacity, with multiple product launches from customers' pipelines—Nvidia's Rubin, AMD's MI400 series/Venice CPU and other cloud ASICs—translating into foreseeable, strong testing demand.

Figure 1: Testing consumables TAM to continue to climb in the next 5 years



Source: Yole, UBS

Executive Summary

Figure 2: Summary of our investment thesis for HTSI, CHPT, and WinWay

Company	Value Chain Positioning	Primary Product Focus	Investment Thesis	Price Target	Upside
Hermes Testing Solutions (HTSI)	Wafer-level Test	Semiconductor testing related installation and services, customized equipment (e.g. thermal control modules for probers), engineering services (CPO test equipment), probe cards.	A key semiconductor testing solution provider and a shift-left beneficiary, with thermal management capabilities that positions the company in the center of AI/HPC chip probing. Uniquely positioned with CPO exposure through its engineering expertise and partnership with ficonTEC.	**NT$8,880**	
Chunghwa Precision Test (CHPT)	Wafer-level Test, Final Test, System-level Test, Burn-in Test	Semiconductor test PCB, final test load board (interface board), probe cards, burn-in board.	A key semiconductor test PCB maker with unique vertical integration capabilities for fast product cadence to enable design-wins. Probe card business is benefiting from the shift-left trend, driving robust growth with design-wins from projects such as CPU and AI ASICs.	**NT$5,000**	
WinWay Technology	Wafer-level Test, Final Test, System-level Test, Burn-in Test	Final test sockets, system-level test sockets, probe cards.	Leading semiconductor test socket provider, beneficiary of final test and mission-level test content expansion with advanced packaging and chiplet proliferation. With its partnership with Technoprobe, WinWay's probe card strength is adding another leg of growth.	**NT$8,900**	

Source: UBS estimates

Shift-left igniting secular growth for chip probing

With the industry increasingly adopting shift-left testing, chip probing (CP) and its supply chain should be key beneficiaries of a multi-year structural growth trend. This underpins our above-consensus forecasts for **Chunghwa Precision Test (CHPT)**, with 2027E/28E sales 7%/15% above consensus driven by stronger AI/HPC demand, capacity expansion, and rising value-added content. **WinWay** should also benefit through its partnership with Technoprobe, with probe card revenue growth remaining robust at 94%/72% in 2026E/27E following 161%/260% growth in 2024/25.

Hermes Testing (HTSI) should be another major beneficiary as increasing chip power and complexity drive demand for advanced thermal-management modules used alongside high-end probing systems. With TEL's leading AI-oriented probers typically paired with advanced thermal-control solutions, we expect HTSI's thermal-module shipments to reach 3,000 units in 2027E from 1,200 in 2026E. Combined with testing, installation and service revenue, this should drive HTSI sales growth of 127%/152% in 2026E/27E.

Accelerators still in focus with TPU as another significant growth driver

Nvidia remains a key growth driver for both CHPT and WinWay. We expect both companies to gain share with Rubin, with WinWay's socket share improving from roughly 50% historically to 60% with Rubin, while CHPT is positioned to supply around 70% of probe card and final test PCB content. Nvidia currently accounts for roughly 50% of WinWay's revenue and 30% of CHPT's.

Beyond Nvidia, we view Google's TPU roadmap as a meaningful incremental opportunity. Following the successful ramp of TPU v8t with MediaTek as design partner, **CHPT** is positioned to supply probe card PCBs, final test load boards, system-level test boards and burn-in boards. **WinWay** will supply sockets for both TPU v8t and v9, with the larger v9 package providing another growth leg. We estimate production of 4mn TPU v8t units in 2027E and 2.3mn TPU v9 packages (9.2mn dies) alongside 2m v8t units in 2028E.

CPU business as a supplemental catalyst for test interface in an agentic world

With agentic AI proliferation, CPU demand is increasing significantly and this directly correlates to increasing demand for testing consumables. WinWay and CHPT should both benefit from the strong ramp up of Nvidia's ARM based Vera CPU and Google's ARM based Axion CPU in 2026E and 2027E. WinWay will be supplying sockets and probe cards for Vera and Axion, and CHPT will be the probe card and PCB supplier for both Vera and Axion. WinWay will have the additional upside from AMD's x86 Venice CPU, and CHPT could capture some share through AMD's equipment vendor procurement. We estimate **CHPT**'s CPU related sales to be low to mid-teens % of total sales in 2026E and growing to 20-30% in 2027E with CHPT's share expansions with turnkey probe card solutions for Google's Axion. For **WinWay**, we believe CPU should account for around 30% of sales in 2026E/27E.

CPO testing fuelling future growth for semiconductor testing

ficonTEC's 25 years of precision optical-test expertise makes it an early leader in CPO test equipment, particularly in optical alignment, a critical capability for high-volume manufacturing. Through its partnership with ficonTEC, **HTSI** is well positioned to benefit from the initial CPO ramp in 2027E-28E by supporting manufacturing scale-up.

We expect both insertion 2 and insertion 3 testing to be required over the next two years. Despite the technical challenges of double-sided wafer probing, insertion 2 testing remains important given current optical-engine yields and the need to identify known-good optical engines before fibre-array-unit (FAU) coupling. This becomes increasingly critical as switch designs integrate larger numbers of optical engines.

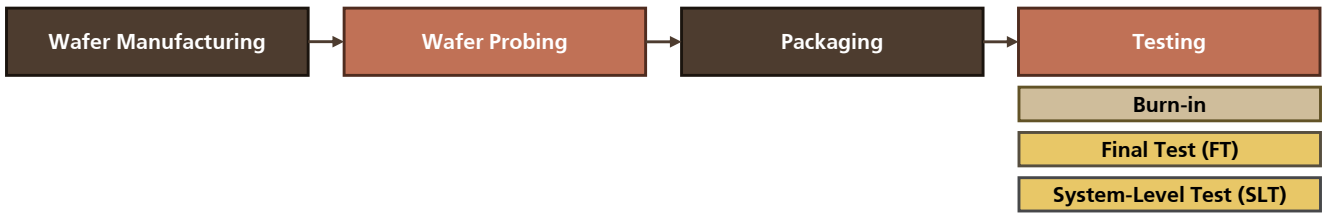
We estimate HTSI will ship 40 insertion 2 and 70 insertion 3 systems in 2027E, with further upside in 2028E as CPO adoption expands and next-generation platforms move into volume production.

Testing TAM expanding with IC complexity: leaders likely to outperform industry growth

Our central view is that testing content per AI accelerator is growing faster than semiconductor unit volumes, creating a multi-year expansion in testing TAM. We believe semiconductor testing is entering a period of structural growth as AI-driven chip complexity increases testing intensity across wafer, package and system levels. The industry's shift-left strategy, which moves more testing upstream in the semiconductor manufacturing process, is resulting in longer and more frequent test insertions. As cloud AI GPUs and ASICs become increasingly complex, additional testing is required to ensure functionality, performance and yield, while reducing defective parts per million (DPPM). More robust testing should improve deployment efficiency and lower the cost of operating AI infrastructure.

Semiconductor testing generally comprises four stages: wafer/chip probing (CP), final test (FT), system-level test (SLT), and burn-in. CP is conducted at the wafer-level before packaging, while FT, SLT, and burn-in occur after packaging. The below Figure 3 illustrates the semiconductor manufacturing flow.

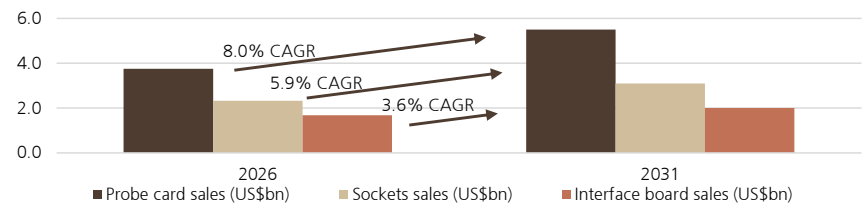
Figure 3: Semiconductor testing process: from wafer level to package level



Source: UBS

We estimate semiconductor testing historically accounts for ~1% of total semiconductor revenue. Within testing, consumables such as probe cards, sockets and interface boards represent ~10-15% of industry revenue. According to Yole, the probe card, socket and interface board markets should grow from US$3.8bn, US$2.3bn and US$1.7bn in 2026 to US$5.5bn, US$3.1bn and US$2.0bn by 2031, respectively.

Figure 4: Yole estimating testing consumables TAM to climb in the next 5 years



Source: Yole, UBS

Nonetheless, leaders within the testing sector are likely to stand out among competition with greater sales CAGR comparing to the industry. Below we highlight **Hermes Testing (HTSI)**, **Chunghwa Precision Test (CHPT)**, and **WinWay**'s impressive growth drivers and how this compares with broader industry sales CAGR.

We see **HTSI**'s sales for the next few years to mainly be driven by 1) thermal control module shipment and 2) CPO equipment shipment. In the past, thermal control modules weren't necessary for chip probing, due to less TDP for the chips. However, as new iterations of AI accelerators now have substantial power draw, this unlocks a brand new TAM for HTSI to enter with their thermal control modules to pair with probers, in order to prevent probe card damage.

- **Robust thermal control module shipments.** We estimate HTSI to ship 3,000/4,100 thermal control modules in 2027E/28E, with continuous demand in future years, bringing their 2026-31E semiconductor equipment sales CAGR to 48%.
- **Thermal control module ASP expansion.** Gen 2 thermal control modules should start to ship in 2027E which will drive tool ASP up around 25-50%.
- **Demand supported by Advantest expansions.** We believe the 3,000 thermal control modules shipment forecast for 2027E is not far-fetched, as we read-across from Advantest's announced capacity expansion plan (testers will be paired with probers with a 1:1 ratio) with increasing capacity up to 5,000 testers within FY2027/3 and they also announced a 10,000-unit target within CY2028. Although the testers capacity expansion plan includes testers for final test, we do see a good portion to be allocated to chip probing given the shift-left testing trend increasing both testing insertions and testing time before chip packaging.
- **CPO is another brand new TAM for semiconductor testing.** As insertion 2 and 3 testing equipment demand starts to rise in 2027E with scale-out CPO adoption, we expect HTSI to ship 40/70 insertion 2 and 3 equipment in 2027E, with this number growing in 2028E to 80/160 and higher in future years as CPO proliferates, and driving 52% 2026-31E test equipment & engineering services sales CAGR.
- **CPO to see content increase.** Gen 2 insertion 3 equipment may start to ship in 2027E, with higher throughput and tool ASP.
- **Insertion 2 might scale down, but not likely any time soon.** Insertion 2 equipment shipment might come down in 2029E and beyond, as foundries scale-up yield for photonic IC (PIC) in order to lessen the time consuming insertion 2 testing burden.

Figure 5: Hermes Testing is set to benefit with a 46% 2026-31E sales CAGR

Sales by Segments NT$m	2026E	2027E	2028E	2029E	2030E	2031E	2026-31E CAGR
Semiconductor Equipment & Customization products	**$2,815**	**$7,980**	**$13,324**	**$16,061**	**$18,315**	**$20,104**	**48%**
YoY		*183%*	*67%*	*21%*	*14%*	*10%*	
Test Equipment & Engineering services	**$1,480**	**$3,887**	**$7,901**	**$8,887**	**$9,898**	**$11,853**	**52%**
YoY		*163%*	*103%*	*12%*	*11%*	*20%*	
Probe cards and cleaning materials	**$1,210**	**$2,012**	**$3,488**	**$4,270**	**$4,597**	**$4,681**	**31%**
YoY		*66%*	*73%*	*22%*	*8%*	*2%*	
Key products shipment units, ASP, sales	**2026E**	**2027E**	**2028E**	**2029E**	**2030E**	**2031E**	**2026-31E CAGR**
Thermal control module shipment	**1,200**	**3,000**	**4,100**	**4,500**	**4,700**	**4,900**	
Thermal control product blended ASP (NT$m)	$1.9	$2.4	$2.8	$3.0	$3.3	$3.5	
Total sales from thermal control module shipment	**$2,316**	**$7,168**	**$11,417**	**$13,505**	**$15,591**	**$17,067**	**49%**
% of total sales	*42%*	*52%*	*46%*	*46%*	*48%*	*47%*	
CPO Insertion 2 shipment	**8**	**40**	**80**	**60**	**20**	**20**	
Ins2 blended ASP (NT$m)	$13.8	$15.8	$17.4	$18.3	$19.2	$20.1	
Total sales from insertion 2	**$111**	**$633**	**$1,391**	**$1,095**	**$383**	**$402**	**29%**
% of total sales	*2%*	*5%*	*6%*	*4%*	*1%*	*1%*	
CPO insertion 3 shipment	**11**	**70**	**160**	**200**	**240**	**280**	
Ins3 blended ASP (NT$m)	$16.0	$17.2	$18.2	$19.1	$20.1	$21.1	
Total sales from insertion 3	**$176**	**$1,202**	**$2,917**	**$3,829**	**$4,824**	**$5,910**	**102%**
% of total sales	*3%*	*9%*	*12%*	*13%*	*15%*	*16%*	
Key product sales - total	**$2,602**	**$9,002**	**$15,725**	**$18,429**	**$20,798**	**$23,379**	**55%**
% of total sales	*47%*	*65%*	*64%*	*63%*	*63%*	*64%*	
Others - total	**$2,903**	**$4,877**	**$8,988**	**$10,789**	**$12,012**	**$13,260**	**36%**
% of total sales	*53%*	*35%*	*36%*	*37%*	*37%*	*36%*	
Operating Metrics	**2026E**	**2027E**	**2028E**	**2029E**	**2030E**	**2031E**	**2026-31E CAGR**
Revenue NT$m	**$5,505**	**$13,879**	**$24,713**	**$29,218**	**$32,810**	**$36,639**	**46%**
YoY		*152.1%*	*78.1%*	*18.2%*	*12.3%*	*11.7%*	
GM %	**55.5%**	**58.3%**	**60.0%**	**60.9%**	**61.3%**	**61.1%**	
OpM %	**19.5%**	**44.3%**	**47.0%**	**48.9%**	**49.3%**	**51.1%**	

Source: UBS estimates

Uniquely positioned as a company with vertical integration capabilities with MEMS probes, multi-layer PCB capabilities, and automation equipment all-in-house, **CHPT** is set to capture the growing test shift-left trend in the coming years, increasing both testing insertions and testing time before chip packaging.

- **CP to scale from a lower base.** As a smaller probe card vendor, CHPT can benefit from the growing demand for AI probe cards, with 2026-31E sales CAGR for turnkey probe card robust at 41%.
- **Also a FT/SLT/burn-in beneficiary.** The company will also see final test, system-level test, burn-in content increase to play a role in their sales growth from their IC Test Board sales CAGR of 39% in 2026-31E.
- **Capacity expansion supporting growth.** As CHPT is currently capacity constrained, the robust projected sales growth is enabled by CHPT's rapid capacity expansion strategy with strong demand for its products, with one production expansion scheduled for August 2026 and a second in March 2027, doubling and tripling year-end 2025 capacity, respectively. Its Fab 3 will come online in Q428, doubling existing capacity when fully ramped.
- **MEMS capability to support share gain.** CHPT has MEMS probe capabilities stemming from its history as a smartphone application processor (AP) probe card supplier. It is in a good position to capture the growing demand for MEMS probe cards as AI/HPC are shifting to MEMS probes.
- **Probe card content expect to rise.** We also expect probe card content per device to continue rising as AI accelerators grow in die size, pin count, power consumption and packaging complexity. This should drive secular growth for both probe card suppliers and upstream component providers, making chip probing one of the most attractive areas within the semiconductor testing value chain.

Figure 6: CHPT is set to benefit with a 35% 2026-31E sales CAGR

Sales by Segments NT$m	2026E	2027E	2028E	2029E	2030E	2031E	2026-31E CAGR
Probe Card	$1,753	$2,903	$4,535	$7,194	$8,361	$9,711	41%
YoY		*66%*	*56%*	*59%*	*16%*	*16%*	
Board Only	$3,574	$6,420	$8,836	$12,650	$13,899	$14,528	32%
YoY		*80%*	*38%*	*43%*	*10%*	*5%*	
Chip Probing	$5,327	$9,324	$13,371	$19,844	$22,261	$24,239	35%
YoY		*75%*	*43%*	*48%*	*12%*	*9%*	
IC Test Board	$1,315	$2,520	$3,579	$5,005	$5,996	$6,825	39%
YoY		*92%*	*42%*	*40%*	*20%*	*14%*	
Service and Others	$502	$640	$918	$1,137	$1,308	$1,504	25%
YoY		*28%*	*43%*	*24%*	*15%*	*15%*	
Operating Metrics	**2026E**	**2027E**	**2028E**	**2029E**	**2030E**	**2031E**	**2026-31E CAGR**
Revenue NT$m	$7,144	$12,484	$17,868	$25,985	$29,565	$32,567	35%
YoY		*74.7%*	*43.1%*	*45.4%*	*13.8%*	*10.2%*	
GM %	56.4%	56.1%	56.2%	56.4%	56.3%	56.3%	
OpM %	35.3%	41.5%	44.0%	45.2%	47.1%	47.3%	

Source: UBS estimates

As the leader in AI/HPC sockets, **WinWay** is set to deliver 2026-31E socket sales CAGR of 33%, underpinned by robust demand for final test and system-level test; with test content and test times rising which each iteration of new AI accelerators/CPU, more sockets and equipment will be needed in order to increase the throughput.

- **Strong accelerator/CPU roadmap to support growth.** Robust testing demand can also be inferred from AI accelerator/CPU roadmaps of Nvidia, AMD, Google, alongside tester capacity expansions by Advantest.
- **Capacity expansion underpinning future strength.** WinWay's socket pin capacity expansion will support this exceptional sales growth. from 3.5mn pins per month at year-end 2025 to 6mn currently, reaching 9mn by year-end 2026 and 14mn by year-end 2027 through expansions in Renwu, Kaohsiung. By 2027, approximately 60% of pogo-pin requirements should be internally sourced, strengthening both supply security and margins.
- **Probe card business to rise from smaller base.** Its probe card business is also set to benefit from the shift-left trend for high-end AI/HPC probe cards. WinWay leverages its existing customers' demand in addition to their MEMS partnership with Technoprobe, as we forecast WinWay's probe card sales to rise from a low base, with a 33% 2026-31E sales CAGR.

Figure 7: WinWay is set to benefit with a 33% 2026-31E sales CAGR

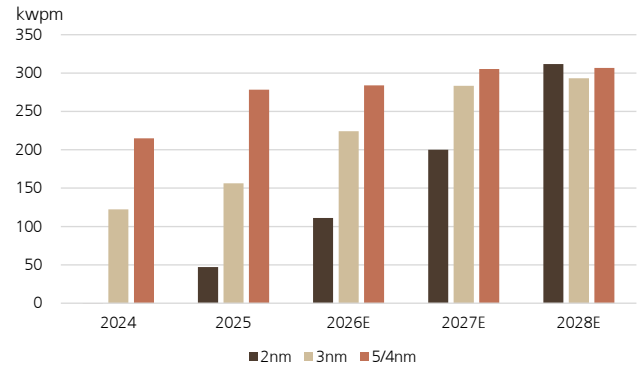
Sales by Segments NT$m	2026E	2027E	2028E	2029E	2030E	2031E	2026-31E CAGR
Coaxial Socket (HyperSocket)	$7,661	$13,705	$23,103	$25,872	$30,603	$34,726	35%
YoY		*79%*	*69%*	*12%*	*18%*	*13%*	
RF & Plastic Socket	$2,311	$3,835	$6,465	$6,960	$7,259	$7,252	26%
YoY		*66%*	*69%*	*8%*	*4%*	*0%*	
Burn-in Socket	$253	$306	$516	$715	$903	$1,075	34%
YoY		*21%*	*69%*	*39%*	*26%*	*19%*	
Test Socket	$10,224	$17,845	$30,083	$33,547	$38,764	$43,053	33%
YoY		*75%*	*69%*	*12%*	*16%*	*11%*	
Probe Card	$4,478	$7,700	$13,690	$15,507	$16,095	$18,403	33%
YoY		*72%*	*78%*	*13%*	*4%*	*14%*	
Contact Element	$937	$1,596	$2,691	$3,014	$3,465	$3,899	33%
YoY		*70%*	*69%*	*12%*	*15%*	*13%*	
Others	$444	$811	$1,367	$1,671	$2,133	$2,654	43%
YoY		*83%*	*69%*	*22%*	*28%*	*24%*	
Operating Metrics	**2026E**	**2027E**	**2028E**	**2029E**	**2030E**	**2031E**	**2026-31E CAGR**
Revenue NT$m	$16,084	$27,952	$47,831	$53,739	$60,457	$68,010	33%
YoY		*73.8%*	*71.1%*	*12.4%*	*12.5%*	*12.5%*	
GM %	41.1%	43.1%	44.7%	44.7%	44.9%	45.1%	
OpM %	27.5%	32.1%	36.7%	36.7%	36.9%	37.1%	

Source: UBS estimates

The AI era has materially increased the value of semiconductor testing. Compared with traditional mobile and automotive chips, AI accelerators incorporate larger compute dies, more advanced nodes, chiplet architectures, advanced packaging technologies, multiple I/O dies, and increasing HBM content. These factors drive higher-value test consumables, including advanced MEMS probe cards, multilayer interface boards, and next-generation sockets designed to support higher pin counts, thermal loading, and power delivery requirements.

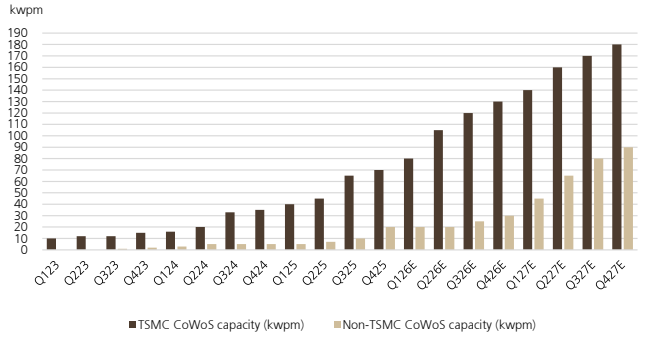
New iterations of semiconductors, especially for AI / HPC applications, are set to increase in both front-end wafer fabrication advancements and back-end packaging complexities with each iterations (i.e. Nvidia's roadmap from Blackwell to Rubin to Feynman or Google's TPU roadmap from v7 to v8 to v9). This trend is evident with TSMC's front-end and TSMC, Intel, and OSAT's back-end advanced packaging capacity expansions. For front-end, we see industry N3 capacity expanding from 156kwpm in year end 2025 to 224/283/293kpwm in year end 2026E/27E/28E, and N2 capacity from 47kwpm in year-end 2025 to 111/200/312kpwm in year end 2026E/27E/28E. For back-end, we are seeing industry CoWoS capacity rising from 90kwpm in 2025 to 160kwpm in 2026E and further expanding to 270kwpm in 2027E.

Figure 8: Industry's leading edge capacity



Source: UBS estimates

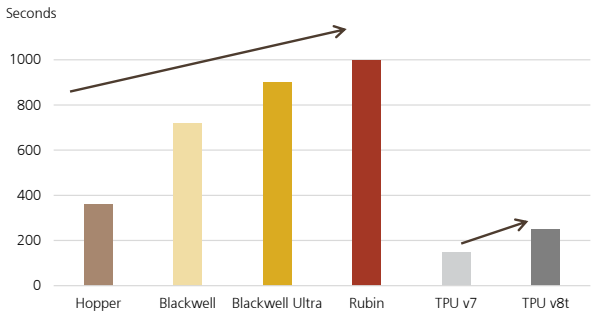
Figure 9: Industry CoWoS capacity



Source: UBS estimates

Final-test, system-level test, and burn-in content should continue to increase as AI accelerators become larger, more power-hungry and more complex. Rising thermal design power and packaging complexity increase validation requirements, driving longer test times and higher demand for test equipment to prevent testing from becoming a production bottleneck.

Figure 10: Our FT test time estimates



Source: UBS estimates

While architectural changes can affect test requirements for individual product generations, we expect the long-term trend of rising testing content to remain intact. For example, Nvidia's Rubin Ultra adopts a simpler package structure than previously expected, from a 4-die structure to a 2-die structure and Rubin Ultra HBM de-spec from HBM4E 12-Hi to initially use HBM4 8-Hi and upgrade to HBM4E 8-Hi at the latter stages, which may moderate near-term test growth. However, future products such as Nvidia's Feynman are expected to reintroduce greater package complexity, with a four-GPU per package structure. More importantly, any reduction in test time can be offset by higher production volumes, making throughput requirements equally important for testing demand.

A rising test trend that lifts all test interface vendors

Figure 11: Key vendors for each stage of the semiconductor testing industry

	Chip Probing	Final Test	System-Level Test
Testing service providers	TSMC, ASE, KYEC, Amkor, Intel	ASE, Amkor, KYEC, JCET, Tianshui Huatian, Tongfu	ASE, Amkor, KYEC, JCET, Tianshui Huatian, Tongfu
Testers	Advantest, Teradyne	Advantest, Teradyne	N / A
Handlers (Probers)	TEL, Tokyo Seimitsu, TSK	Advantest, Chroma, Cohu, Hangzhou Changchuan Technology, Hon Precision, JHT, Teradyne	Hon Precision, Chroma
Probe Cards	FormFactor, Technoprobe, MPI, MJC, JEM, WinWay, CHPT	N / A	N / A
Socket	N / A	WinWay, Cohu, Leeno, Yokowo, Yamaichi, Smiths	WinWay
Load board	N / A	Yamaichi, Advantest, CHPT	Yamaichi, Advantest, CHPT

Source: UBS

Below we summarize key technical items of probe cards, sockets, and load boards/PCB used for semiconductor testing:

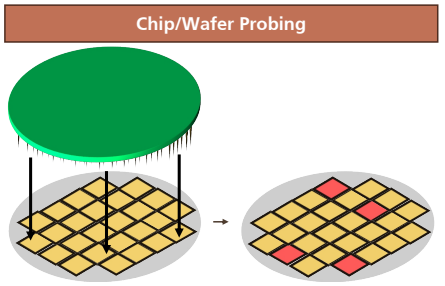
Probe cards and chip probing (CP)

Probe cards are used during chip probing (CP), the wafer-level stage of semiconductor testing that identifies known-good dies (KGD) before packaging. As advanced packaging technologies such as CoWoS, 3D stacking and hybrid bonding become more prevalent, CP is becoming increasingly important because a single defective die or HBM stack can compromise the entire package. This is driving the industry's shift-left testing strategy, with more testing conducted earlier in the manufacturing process to identify defects before costly packaging steps.

Probe cards consist of contact elements (probes) mounted on a PCB and are used together with probers and automated test equipment (ATE). During testing, wafers are placed on the prober chuck while the probe card makes electrical contact with individual dies. The tester then performs electrical, parametric, and functional tests to determine whether each die meets performance requirements. Dies that fail testing are removed from the production flow prior to dicing and packaging.

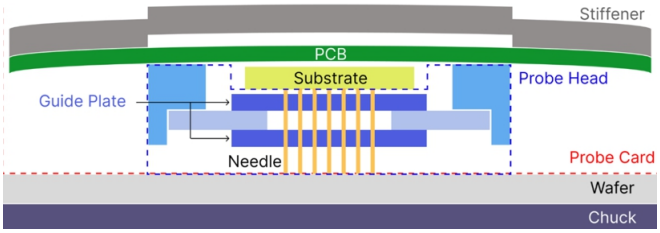
Furthermore, probe cards are highly customised products designed for specific chip architectures and testing platforms. As AI accelerators adopt larger dies, higher pin counts and more advanced packaging technologies, probe card complexity and content value continue to increase.

Figure 12: Chip probing utilise probe cards to find known-good dies (KGD) and eliminate faulty dies



Source: UBS

Figure 13: CP test illustration with probe card structure

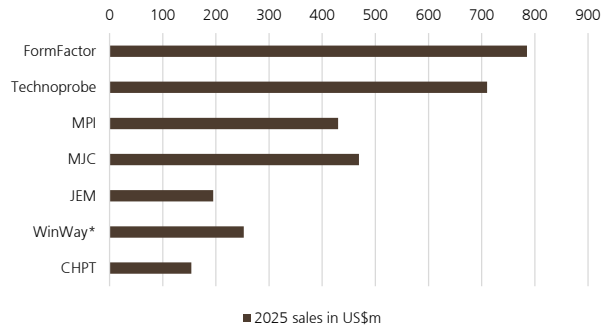


Source: Company data (CHPT)

The global probe card market remains concentrated among a handful of suppliers:

- **FormFactor (FORM.O)**: World's largest probe card company (including both logic and memory probe cards) by revenue as of year end 2025. Key supplier for HBM probe cards.
- **Technoprobe (TPRO.MI)**: World's largest logic probe card company by revenue as of year end 2025. Key supplier for AI accelerators MEMS probe cards, especially for GPU.
- **MJC (6871.T)**: Japanese company, mainly specializing in memory probe cards, 3rd largest probe card company by revenue as of year end 2025.
- **MPI (6223.TWO)**: Traditionally specializes in cantilever probe cards, now expanding its MEMS probe capacity. 4th largest probe card company by revenue as of year end 2025. A probe card supplier of AI ASICs.
- **JEM (6855.T)**: Mainly specialize in memory probe cards, 5th largest probe card company by revenue as of year end 2025.
- **WinWay (6515.TWO)**: One of the fastest-growing logic probe card suppliers. Following its collaboration with Technoprobe, WinWay rose from the 15th-largest probe card supplier in 2024 to the fifth-largest logic probe card supplier in 2025. Probe card revenue increased from 11% of sales in 2024 to 29% in 2025.
- **Chunghwa Precision Test Tech (6510.TW)**: A key supplier for smartphone application processor (AP) probe cards, and has been migrating to HPC related applications in recent years. Although its share within the probe card market is minor, it is a major supplier for probe card PCB, especially for high end probe cards with advanced PCB that has high layer counts (>40 layers, and over 80 layers for AI applications). Its key competitive advantage is its vertical integration as it manufacturers the MEMS probe and PCB in-house.

Figure 14: 2025 sales of major probe card suppliers



Source: Company data, UBS. Note: Only 29% of WinWay's 2025 sales are from probe cards.

Probe cards generally employ either **vertical** or **cantilever** architectures. **Vertical** probe cards use probes arranged perpendicular to the substrate, enabling higher pin density

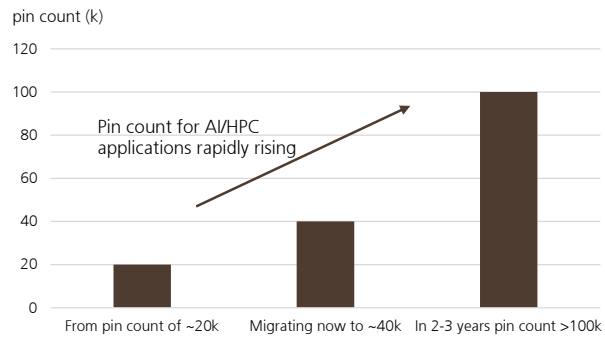
and finer pitch capability. They have become the standard for AI, HPC and other advanced semiconductor applications. **Cantilever** probe cards use angled probes extending from the PCB and are typically used in analog, driver IC and selected memory applications where pin-count and pitch requirements are less demanding. The latest generation of AI accelerators increasingly relies on **MEMS** (Micro-Electro-Mechanical Systems) based vertical probe cards, which support ultra-fine pitches, higher pin counts and improved probing precision. Technoprobe currently leads this segment with pitch capability reaching approximately 40 micrometres.

For leading-edge AI applications, probe cards must increasingly support:

1. Higher current-carrying capability (CCC).
2. Stable contact resistance.
3. Lower parasitic inductance for signal integrity.
4. Greater durability under varying thermal conditions.

For **CHPT**, with their MEMS probe capabilities stemming from their smartphone application processor probe card supply, they are in a good position to capture the growing demand for MEMS probe cards as AI/HPC are shifting to MEMS probes. We also expect probe card content per device to continue rising as AI accelerators grow in die size, pin count, power consumption and packaging complexity. This should drive secular growth for both probe card suppliers and upstream component providers, making chip probing one of the most attractive areas within the semiconductor testing value chain.

Figure 15: Probe card pin count growth trajectory

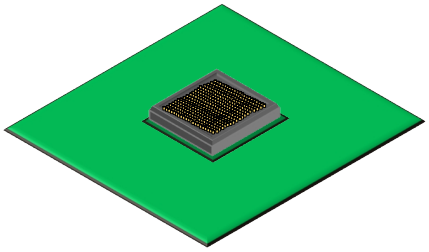


Source: UBS estimates

Sockets

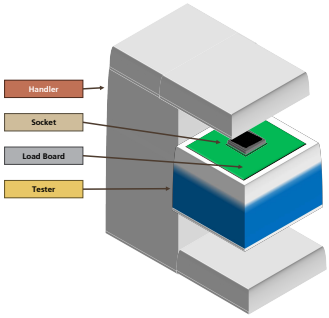
Semiconductor test sockets are electro-mechanical interfaces that are used post chip probing and chip packaging process to test the functionality of the chips. Sockets are placed on to load boards on top of testers during the final test/system level test processes. Handlers place the chips onto the sockets, and pins inside the sockets enable the testers to read the signals from the device under test (DUT, i.e. the packaged chips), with tester signals fanning out from beneath the PCB load board.

Figure 16: Socket illustration



Source: UBS

Figure 17: FT equipment/ consumables



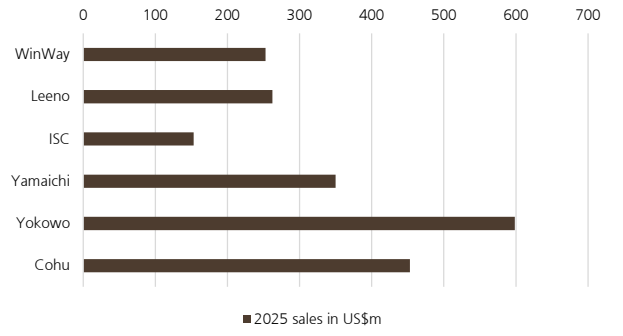
Source: UBS

As AI accelerators become larger and more complex, socket requirements continue to increase. High-end sockets typically comprise a socket housing, alignment plate, integrated thermal-control components and contact elements that connect the DUT to the tester. Spring probes (pogo pins) are the most common choice for HPC sockets, with high durability, individual probe replacement flexibility, and consistent contact force. FT and SLT sockets account for more than 70% of the total socket market, with burn-in sockets representing the remainder.

Compared with the probe card market, the socket industry is more fragmented. Key suppliers include:

- **WinWay (6515.TW)**: A major share gainer in AI/HPC sockets, with strong exposure to Nvidia and AMD. The company specializes in high-performance coaxial sockets and is developing its next-generation HyperSocket platform. It is also expanding into probe cards through its partnership with Technoprobe.
- **Leeno (058470.KQ)**: Vertically integrated supplier focused on smartphone AP and memory sockets.
- **ISC (095340.KQ)**: Leading memory socket supplier with elastomer expertise.
- **Smiths Interconnect (Acquired by Molex)**: A key player in AI/HPC socket industry, with its DaVinci coaxial sockets able to support high frequency connectivity testing.
- **Yamaichi (6941.T)**: Leading Japanese socket supplier with strong automotive exposure.
- **Yokowo (6800.T)**: Major provider of contact probes and socket pins.
- **Cohu (COHU.O)**: Broad test-solutions provider spanning ATE, handlers and sockets, with greater auto/industrial/consumer exposure.

Figure 18: 2025 sales of major socket suppliers



Source: Company data, UBS. Note: Most socket suppliers are companies with multiple business segments, i.e. Yokowo and Cohu.

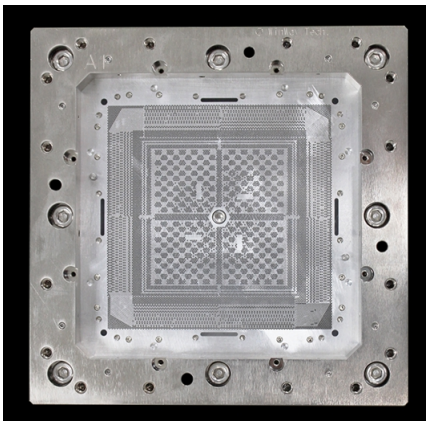
AI accelerators are pushing socket requirements beyond 10,000 pins, making **coaxial sockets** the industry standard for leading-edge AI/HPC devices. These sockets must support transmission speeds of up to 224G while handling significantly higher thermal design power (TDP) during testing.

Elastomer technology is increasingly being adopted alongside spring-probe (pogo-pin) architectures to reduce chip damage and improve contact reliability. WinWay's next-generation **HyperSocket** integrates elastomer materials between the DUT and spring probes, improving probe lifetime, reducing cleaning requirements and enhancing production efficiency. We believe HyperSocket could become an important differentiator as next-generation AI accelerators demand higher pin counts, bandwidth and thermal performance. We estimate HyperSocket could contribute approximately 5% of WinWay's revenue in 2027E while carrying a 20-30% ASP premium versus conventional coaxial sockets.

The transition toward larger AI packages, higher pin counts and faster data-transfer speeds should continue to increase socket content per device. We expect this trend to support long-term growth in the socket market, with technology leaders such as WinWay well positioned to gain share through next-generation solutions including

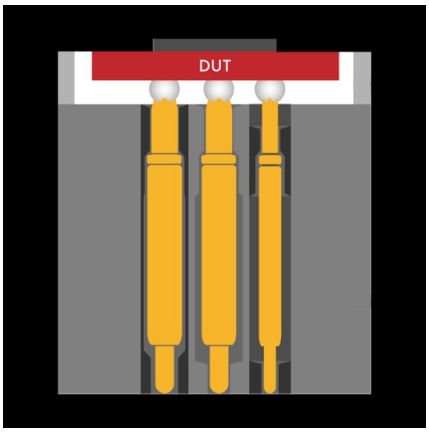
HyperSocket.

Figure 19: Coaxial socket



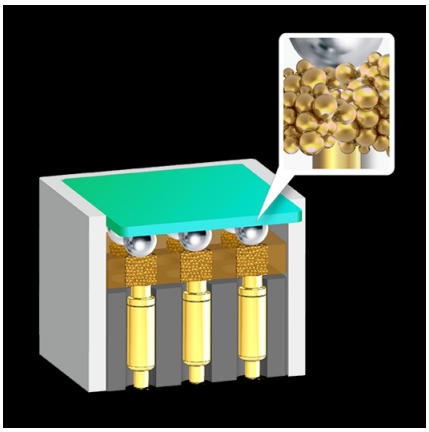
Source: Company data (WinWay)

Figure 20: DUT socket contact



Source: Company data (WinWay)

Figure 21: HyperSocket



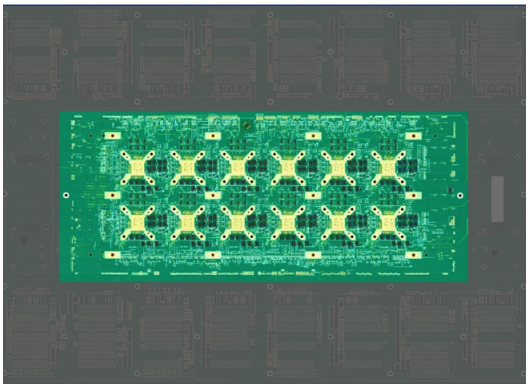
Source: Company data (WinWay)

Load Board/Interface board

Load boards are specialised printed circuit boards (PCBs) that connect the tester to the device under test (DUT) during final test (FT) and system-level test (SLT). Acting as the electrical interface between the packaged chip and automated test equipment (ATE), load boards are responsible for power delivery and high-speed signal transmission throughout the testing process. As AI and HPC devices become increasingly complex, load board requirements continue to rise. **Multilayer construction** is crucial as modern load boards often require more than 50 layers for smartphone application processors and over 80 layers for leading-edge AI accelerators to support higher pin counts, dense signal routing and greater power delivery demands. At the same time, **impedance control** is an important factor as maintaining signal integrity is becoming increasingly important as interconnect bandwidth rises and high-speed SerDes blocks become more prevalent. These trends are driving greater technology content and value per load board.

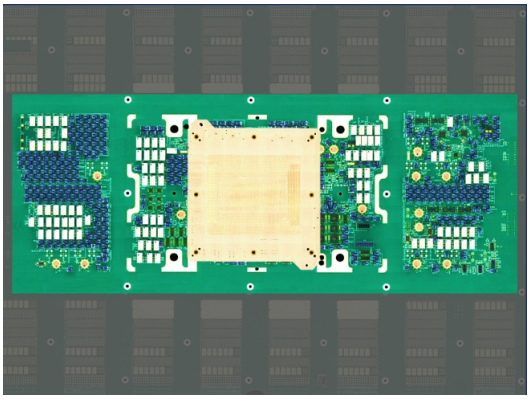
We expect load board content to increase alongside AI chip complexity, larger package sizes and higher interface speeds, benefiting suppliers with advanced multilayer PCB capabilities such as CHPT.

Figure 22: CHPT's AP load board



Source: Company data (CHPT)

Figure 23: CHPT's AI load board



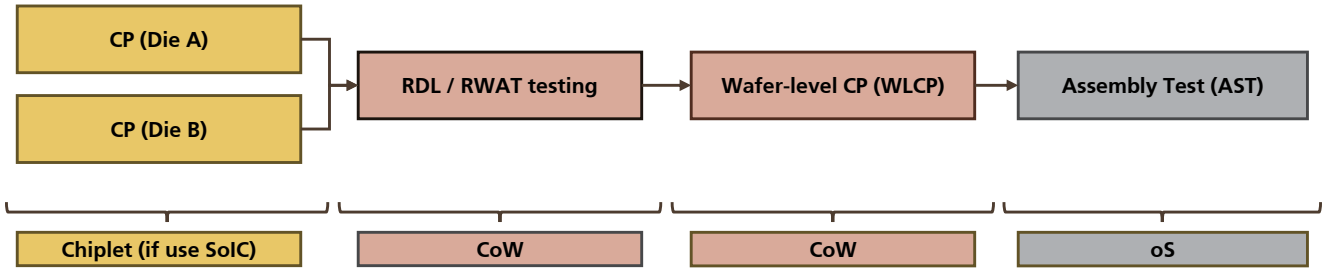
Source: Company data (CHPT)

Shift-left igniting secular growth for chip probing

The industry's adoption of shift-left testing should drive a multi-year structural growth opportunity for chip probing (CP) and its supply chain. As advanced packaging costs rise and AI accelerators become increasingly complex, semiconductor manufacturers are placing greater emphasis on identifying known-good dies (KGD) before packaging. This

underpins our above-consensus forecasts for **Chunghwa Precision Test (CHPT)**, with 2027E/28E sales 7%/15% above consensus driven by structural AI/HPC probe card and test consumables demand, capacity expansion, and increasing test interface content as test insertions and test time increase. **WinWay** should also benefit through its growing probe card business alongside partner Technoprobe, with probe card sales expected to grow 94%/72% YoY in 2026E/27E following 161%/260% growth in 2024/25.

Figure 24: CP is set to grow substantially with shift-left, each packaging step set to be MORE costly than the prior step

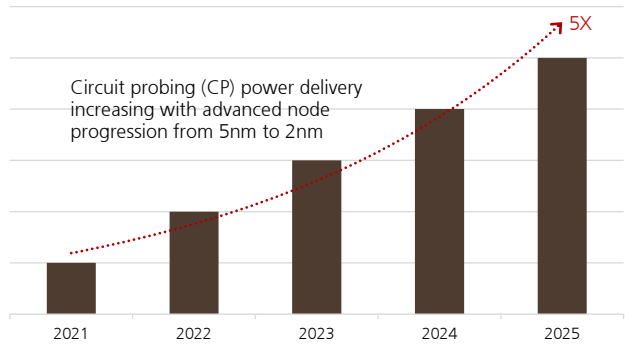


Source: UBS

The economics of advanced packaging reinforce this trend. Heterogeneous integration, chiplet architectures and 2.5D/3D packaging significantly increase package value, while defects identified late in the manufacturing process can lead to substantial scrap costs. To mitigate this risk, foundries and OSATs such as TSMC and ASE employ distributed testing flows incorporating KGD, known-good-stack (KGS) and assembly test screening, to catch defects before the components enter a multi-week packaging cycle (>2 weeks for CoW and 2 weeks for oS). The importance of these tests rises as AI clusters become increasingly dependent on component reliability and low defective-parts-per-million (DPPM) rates. Given the multiplicative yield degradation, a 300bps yield decline at just one manufacturing stage (e.g. dropping from 99.5% to 96.5%) reduces overall integrated four-stage yield from 98.0% to 95.0%; on a 500,000 unit ramp at US $10,000 per unit, this 3% scrap delta translates into around US$150m in unrecoverable losses given >6-month manufacturing lead times.

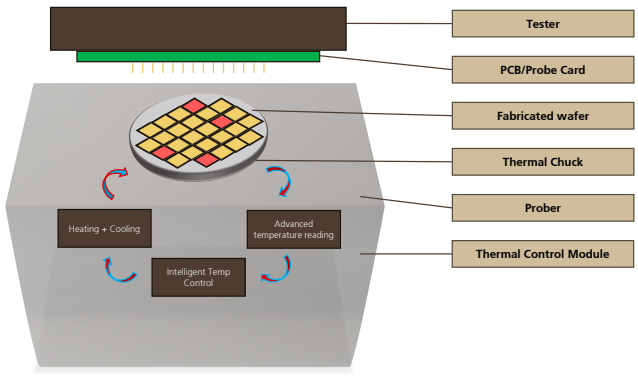
At the same time, rising chip power consumption is increasing the technical difficulty of wafer-level testing. As chip thermal design power scales beyond 1,000W and power density is expected to surge another 8x by 2030, traditional wafer-level chip probe (WLCP) encounters severe physical bottlenecks. Finer probe pitches and higher power densities increase the risk of overheating, probe needle burnout and yield degradation, creating demand for more advanced probing and thermal control solutions.

Figure 25: CP power delivery trend rises with process tech evolution



Source: UBS

Figure 26: Thermal control module inside probers are essential to control wafer temperature



Source: UBS

Hermes Testing (HTSI) is a key beneficiary of this trend. Leveraging its long-standing relationship with TSMC and expertise in semiconductor test solutions, HTSI supplies advanced thermal control modules used alongside leading-edge probers (made by Tokyo Electron), particularly for AI applications. These thermal control modules are

required for high TDP semiconductor wafer probe in order to maintain the temperature of the chuck to avoid needle burns or probe card damages. We estimate HTSI will ship approximately 3,000 thermal-management modules in 2027E, up from 1,200 in 2026E, supporting sales growth of 127%/152% in 2026E/27E. HTSI is also the partner for prober installation, prober maintenance and services. In addition, HTSI provides high-end chuck processing services, an area that should benefit from increasing package sizes and higher wafer warpage associated with advanced packaging.

Beyond thermal control modules, HTSI also supplies consumables and customised solutions for wafer-level testing, including probe card cleaning sheets and laser-based probe head cleaning systems. As probing intensity increases under the shift-left testing model, demand for cleaning and maintenance solutions should rise alongside probe card utilisation. Currently, cleaning sheets is around 5% of sales, but we believe it could gain traction in 2027/28E and beyond. We see additional upside from future modular laser cleaning systems that could be integrated directly with probers, further expanding HTSI's content opportunity within advanced wafer-level testing.

Rapid capacity expansions accelerating growth

Industry test interface suppliers are expanding capacity aggressively to meet rising AI and HPC demand. As advanced semiconductors require higher-performance probe cards, sockets and interface boards, capacity additions are becoming increasingly important to support growth across both wafer-level and package-level testing.

We believe **CHPT** and **WinWay** are well positioned to gain share within the high-end AI/HPC test interface market. Taiwanese suppliers benefit from their proximity to leading fabless customers and the growing preference for localised supply chains, particularly for advanced testing applications where responsiveness and engineering support are critical. Against a backdrop of tight industry supply, both companies have announced significant capacity expansion plans over the next two to three years.

CHPT: capacity expansion supporting AI/HPC share gains

CHPT's existing capacity is effectively fully utilised and the company is pursuing both near-term and long-term expansion. Near-term growth will come from leased facilities, with one production expansion scheduled for August 2026 and a second in March 2027, doubling and tripling year-end 2025 capacity, respectively. Longer term, CHPT's new Fab 3 facility in Pingzhen will significantly expand in-house PCB manufacturing and wet-processing capacity, with mass production expected around Q428, expected to double existing capacity when fully ramped.

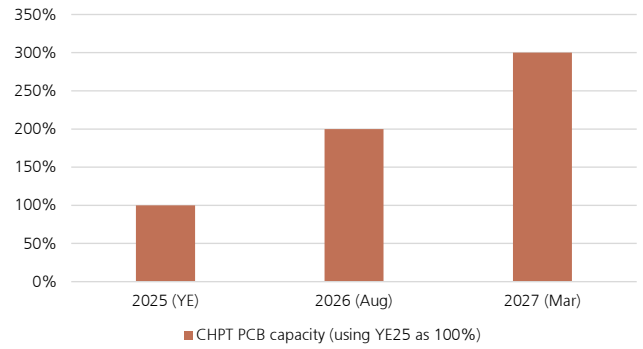
Combined with increasing exposure to higher-value AI/HPC products, including turnkey CPU probe cards and TPU FT/SLT/burn-in boards, we expect CHPT to deliver revenue growth of 49%/75%/43% in 2026E/27E/28E.

WinWay: scaling for the next phase of AI demand

WinWay's capacity is expected to increase from 3.5mn pins per month at year-end 2025 to 6mn currently, reaching 9mn by year-end 2026 and 14mn by year-end 2027 through expansions in Renwu, Kaohsiung. By 2027, approximately 60% of pogo-pin requirements should be internally sourced, strengthening both supply security and margins.

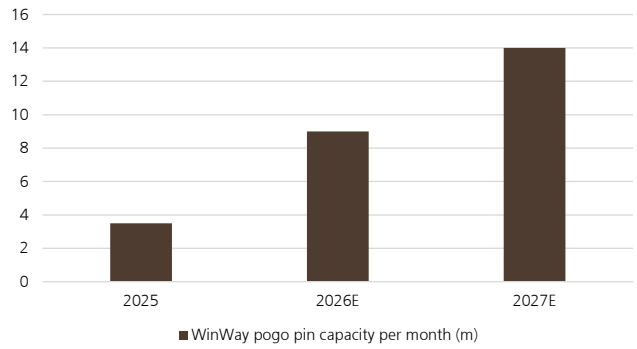
We estimate these capacity additions will support revenue growth of 105%/73%/71% in 2026E/27E/28E.

Figure 27: Announced capacity expansions for CHPT



Source: Company data, UBS

Figure 28: Announced capacity expansions for WinWay



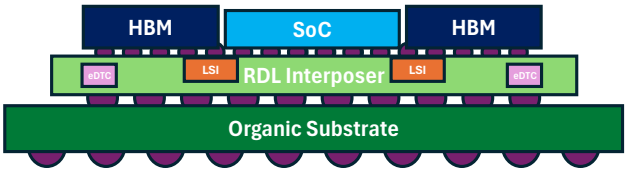
Source: Company data, UBS

Advanced packaging growth remains the key demand driver

Capacity expansion by test interface vendors is ultimately supported by continued investment throughout the advanced packaging ecosystem, from providers such as TSMC, ASE, Intel, and Amkor. During the Q226 earnings calls, TSMC raised its recent 2026 capex from US$52-56bn to US$60-64bn and ASE raised its 2026 capex from US $8.5bn to US$10.5bn, with both companies citing robust demand supporting the capex raise. We believe capex for the next two years will be even higher than 2026, implying continuous growth in future years. With advanced packaging technologies getting significantly more complex and with larger form factor, illustrated by the upcoming ramp of both TSMC's CoPoS (chip-on-panel-on-substrate) and Intel's EMIB-T (embedded multi-die interconnect bridge) packaging technologies, test interface solution providers will benefit with more value added consumables (see our CoPoS vs EMIB-T deep dive).

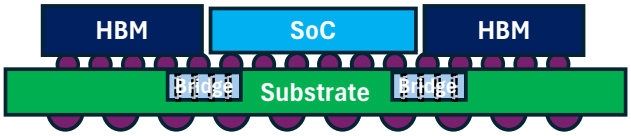
We expect test interface content growth to outpace unit growth. For instance, test socket's ASP directly correlates with its pin counts - with the addition of 20-30% more pins inside the sockets, socket ASP can grow 20-30% or more as the socket might require significant cooling capabilities as the TDP of the DUT rises with its larger form factor. Unlike prior semiconductor cycles, much of the current demand is driven by rising test interface content per device rather than unit growth alone.

Figure 29: TSMC's CoPoS



Source: UBS

Figure 30: Intel's EMIB-T



Source: UBS

Accelerators still in focus with TPU as another significant growth driver

Nvidia has been the primary driver of testing content growth over the past several years, benefiting the entire semiconductor testing supply chain. We expect this trend to continue as GPU architectures evolve from Blackwell to Rubin and then to Feynman, with increasing process node complexity, larger package sizes and more advanced packaging technologies driving higher testing value per device.

Nvidia should remain a major contributor to both CHPT and WinWay, with GPUs continuing to serve as their core growth engine. Both companies are positioned to gain share with Rubin. We estimate WinWay's socket share could improve from a 50/50 split with Smiths Interconnect in prior generations to 60/40 with Rubin, while CHPT is gaining

share in test interface PCBs and is positioned to supply around 70% of Rubin probe card and final test PCB content. Nvidia currently accounts for approximately 50% of WinWay's sales and 30% of CHPT's sales. Both Nvidia GPUs and Google TPUs increase testing demand through higher content per device rather than unit growth alone.

Beyond Nvidia, Google's TPU roadmap represents a significant incremental growth opportunity. Following the successful ramp of TPU v8t with MediaTek as design partner, **CHPT** is positioned to supply probe card PCBs, final test load boards, system-level test boards and burn-in boards. For v9, although the final test interface vendors are yet to be decided, we believe as the current supplier, CHPT will still be supplying PCB for final test, system level test, and burn-in, with potential to continue to supply PCB for probe cards. **WinWay** should also benefit as the socket supplier for both TPU v8t and the next-generation TPU v9 platform. We believe MediaTek's increasing share gain for Google TPUs will also benefit the local Taiwanese test interface supply chain.

We view TPU v9 as a particularly attractive opportunity given its large four-die package architecture based on Intel's EMIB-T packaging technology, which should drive higher testing content. We estimate production of 4mn TPU v8t units in 2027E, followed by 2.3mn TPU v9 packages (9.2mn dies) and an additional 2mn TPU v8t units in 2028E. Importantly, while EMIB-T packaging is expected to be performed in Malaysia, we believe the majority of advanced testing value should remain within the Taiwanese testing ecosystem. Leading testing providers, including ASE and KYEC, maintain substantial testing operations across Taiwan and Southeast Asia, supporting continued participation by Taiwanese test interface suppliers. See our latest MediaTek report.

CPU business as a supplemental catalyst for test interface in an agentic world

We believe semiconductor test interfaces are an underappreciated beneficiary of the emerging agentic AI ecosystem. UBS estimates the CPU market will expand to US $170bn by 2030E from US$31bn in 2025 and US$71bn in 2027E, driven by rising deployment of AI infrastructure. As CPU-to-GPU ratios increasingly approach 1:1 in AI clusters, demand for testing interfaces should expand alongside CPU volumes. TSMC is the main CP test provider in the industry, with probe card suppliers aiding its massive demand by supplying probes, such as TSMC's GPU probe cards supported by Technoprobe's probes. However, with capacity now becoming scarce with strong front and back-end demand, TSMC is outsourcing its CP business to ASE and KYEC, further broadening the testing supply chain. This is where new probe card vendors come in—smaller probe card players in the past, such as **WinWay** and **CHPT**, now have the opportunity to gain significant, non-GPU share from TSMC, as they have MEMS probe capabilities (WinWay's MEMS probes are from its strategic partnership with Technoprobe) and has a long established relationship with the fabless companies such as Nvidia via supplying non-probe card consumables such as sockets and PCB. Of which, CPU projects have become the main area for CHPT and WinWay to expand their footprint.

We expect both companies to benefit from the ramp of Nvidia's ARM-based Vera CPU and Google's ARM-based Axion CPU in 2026E-27E. WinWay is positioned to supply sockets and probe cards for Vera and sockets for Axion, while CHPT should provide probe cards and test interface PCBs for both Vera and Axion, with particularly strong exposure to Axion. Additional upside could come from AMD's Venice CPU, where WinWay is well positioned and CHPT could gain indirect exposure through testing-equipment procurement channels. We estimate CPU-related revenue will represent low to mid-teens % of CHPT sales in 2026E, increasing to 20-30% in 2027E as the company expands its turnkey probe card solutions for Axion. For WinWay, CPU-related demand could account for approximately 30% of sales in 2026E-27E. Importantly, CPU programmes diversify exposure beyond AI GPUs and provide a second structural growth driver for test interface suppliers.

CPO testing fuelling future growth for semiconductor testing

As interconnect bottlenecks increasingly shift from the memory wall to the copper wall, we believe co-packaged optics (CPO) adoption is inevitable over the longer term. Testing remains one of the key bottlenecks to CPO deployment, as optical validation differs

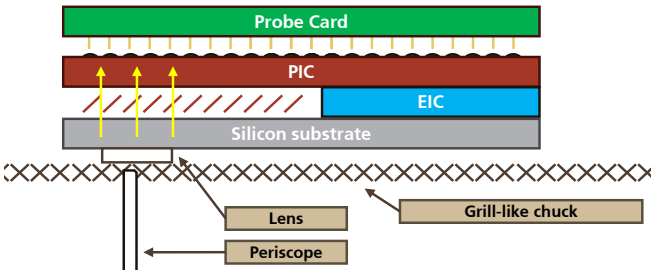
fundamentally from the electrical testing processes that have dominated semiconductor manufacturing for decades. As a result, CPO is creating a new testing opportunity across the semiconductor equipment and consumables ecosystem. We have written extensively on CPO and the opportunities that it brings to the semiconductor supply chain, see our CPO deep dive, our thoughts on CPO timing, 2026 SiPhIA conference takeaways, and SEMICON 2026 takeaways.

Various test equipment suppliers are scrambling to come up with ideal testing equipment across the four insertions of CPO testing, with solutions to ensure both optical and electrical signal integrity of the CPO solutions. The four insertions are:

- **Insertion 1: Electronic IC (EIC)/Photonic IC (PIC) test.** Single-side wafer test that has dedicated probe cards to test the fabricated EIC/PIC wafers.
- **Insertion 2: Optical/Electrical test.** Double sided wafer test, testing the hybrid bonded (e.g. via TSMC's COUPE) EIC and PIC wafers by an opto-electrical test that verifies the electrical signals on the top and optical signal on the bottom of the hybrid bonded wafers.
- **Insertion 3: Optical engine (OE) test.** The OE tests are done to ensure the quality of the OEs and with FAU (Fiber Array Unit) attached, to ensure the signal integrity of the OEs. The testing equipment needs to be able to handle 224G per channel data rates, requiring high unit per hour (UPH) throughput, meticulous dirt mitigation, and maintaining a near 100% contact rating on high-speed sockets.
- **Insertion 4: ASIC final test.** This final test step is established post the OEs are packaged together with the ASIC. The complete ASIC package (now with CPO) is now tested for opto-electrical functionalities.

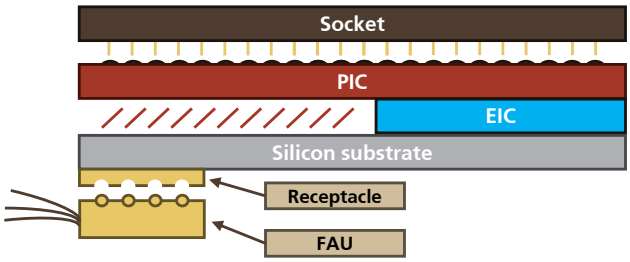
As it stands, insertion 2 and insertion 3 are the two areas where there are the most debates in the industry. Insertion 3 suppliers such as Chroma have noted the trend of "shift-to-middle" paradigm centered on insertion 3. In high-density scale-out switches deploying up to 32 optical engines (e.g. Nvidia's Spectrum-X architectures), any OE defect results in package scrap at the CoWoS level, making 100% known-good die (KGD) validation at the singulated OE stage an absolute commercial requirement.

Figure 31: An illustration for insertion 2 test method



Source: UBS

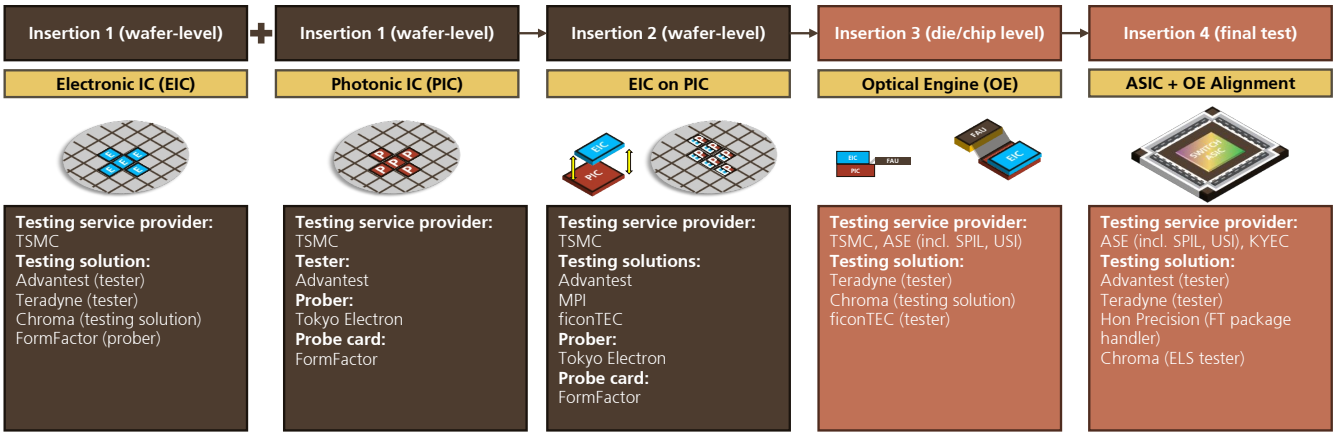
Figure 32: An illustration for insertion 3 test method



Source: UBS

As shown in the below figure, as there are no set standards for the testing equipment, throughput and stability are now the main targets and areas of competition for the major players in the field. Notable ones for each insertions are listed.

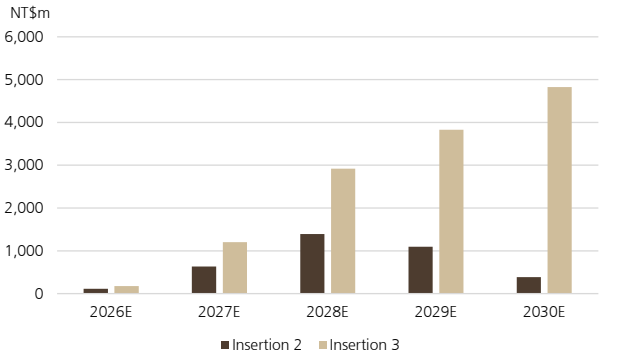
Figure 33: CPO testing flow chart with key suppliers



Source: UBS

With its 25 years of precision test equipment expertise, ficonTEC is an early mover for CPO test equipment and has key know-how for optical alignment, which is quintessential for optical test. **Hermes Testing**, through its partnership with ficonTEC, is set to be a major beneficiary once CPO proliferates in 2027E-28E. As the partner of ficonTEC, Hermes Testing is the key enabler that can help ficonTEC achieve HVM for its CPO testing equipment. As of now, our view is that both insertion 2 and insertion 3 should be required within the next two years, despite the difficulties surrounding double-sided wafer probing (insertion 2), as the yield for OEs is still not high enough to avoid defective dies. Finding out known-good OEs will be crucial before the FAU coupling process during the latter stages of CPO packaging, to prevent impeding the final package with multiple OEs attached to the switch ASIC (e.g. 32 OEs on Nvidia's Spectrum-X). We estimate Hermes Testing will ship 40/70 units of insertion 2/3 testing equipment in 2027E, with upside to these numbers as we view Hermes Testing will likely assist with the ramp up for Gen 2 insertion 3 equipment in 2027E. Gen 2 insertion equipment will come with better throughput and ASP.

Figure 34: HTSI CPO equipment sales to pick up in 2027/28E with 541%/135% YoY growth



Source: UBS estimates

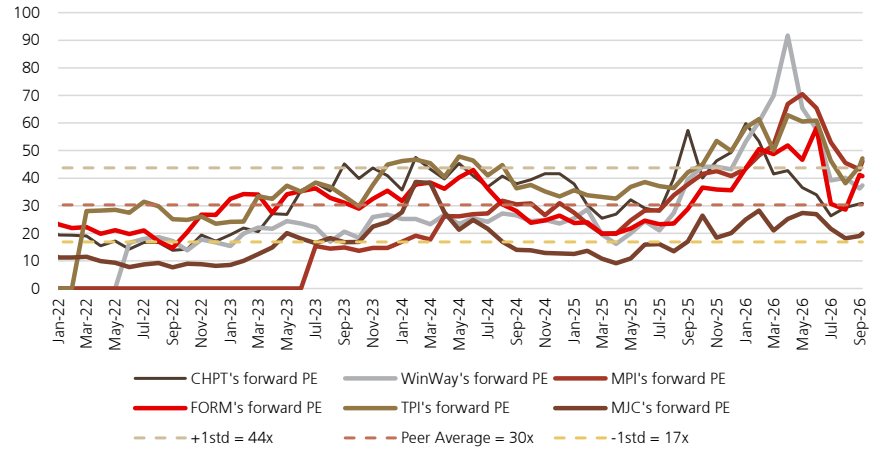
Beyond insertions 2 and 3, HTSI is also positioned to participate in insertion 1 testing through customised prober solutions for photonic integrated circuit (PIC) testing. We believe these solutions could eventually be packaged as licensable intellectual property, creating an additional long-term growth opportunity as CPO adoption broadens. While near-term testing growth is driven by AI accelerators, CPO represents the next major expansion cycle for semiconductor testing. We believe HTSI is uniquely positioned to participate across multiple test insertions, providing exposure to a potentially significant source of incremental revenue beginning in 2027E.

Valuation comparison

We set up three peer groups for valuation comparison: probe card, sockets, and equipment vendors.

For probe card vendors, the peer group's average NTM PE post 2022 is around 30x, and the group is currently trading at around 39x NTM PE. We value CHPT using 31x average 2027-28E PE, in-line with its historical average of 31x and underpinned by a 31% 2027-31E earnings CAGR.

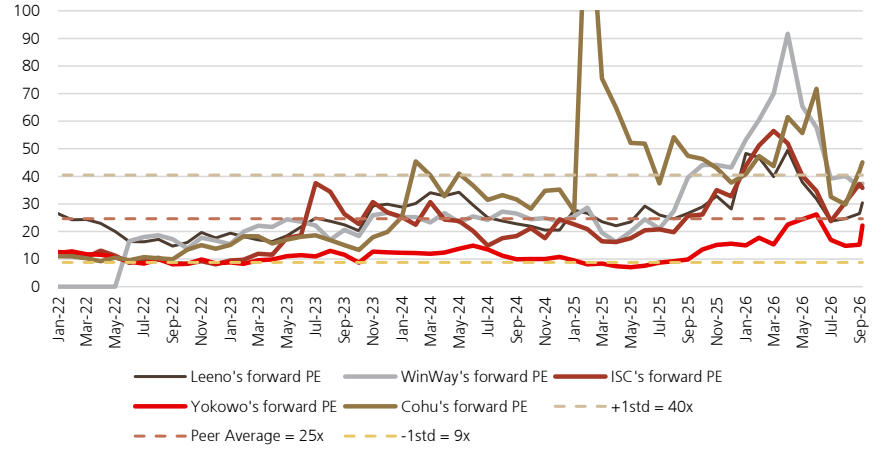
Figure 35: Key probe card vendors' 12-month forward PE band (x)



Source: LSEG, UBS

For socket vendors, the peer group's average NTM PE post 2022 is around 25x, and the group is currently trading at around 39x NTM PE. We value WinWay using 30x average 2027-28E PE, in-line with its historical average of 30x and underpinned by a 30% 2027-31E earnings CAGR.

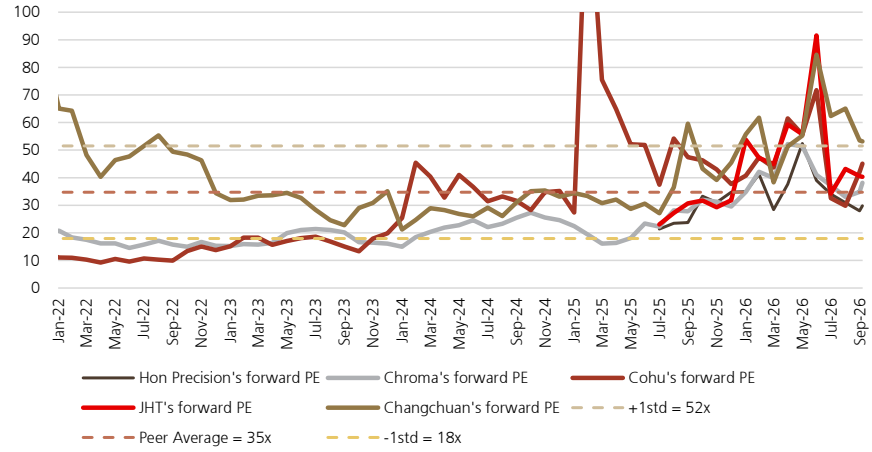
Figure 36: Key socket vendors' 12-month forward PE band (x)



Source: LSEG, UBS

For equipment vendors, the peer group's average NTM PE post 2022 is around 35x, and the group is currently trading at around 41x NTM PE. We value HTSI using 31x average 2028E PE, underpinned by a 32% 2027-31E earnings CAGR. We use 2028 PE as our view is that 2028 is the year thermal control modules and CPO adoption grow from the initial ramping up stage to mass adoption stage. We believe that using handlers as a peer group is justifiable for a unique company like HTSI, with thermal control modules for chip probing sharing similar characteristics to active thermal control used for final test, in addition to Hon Precision and Chroma having exposure to CPO test equipment.

Figure 37: Key equipment vendors' 12-month forward PE band (x)



Source: LSEG, UBS

Figure 38: Testing supply chain valuation table

Company name	Ticker	Analyst	Market cap (US$m)	Price Target (LC)	Share price (LC)	Rating	EPS growth (%)		P/E (x)		P/BV (x)		ROE (%)	
							2026E	2027E	2026E	2027E	2026E	2027E	2026E	2027E
Testing service provider														
ASE Industrial	3711.TW	Sunny Lin	104,043	835	744	Buy	104	64	39.3	24.0	7.5	6.3	21	28
King Yuan Electronics	2449.TW	Sunny Lin	11,456	325	298	Buy	40	62	32.6	20.1	5.9	5.0	20	27
Amkor Technology	AMKR.O	Randy Abrams	13,114	80	53	Buy	73	8	20.6	19.1	2.6	2.4	14	13
JCET Group	600584.SS	Jimmy Yu	17,156	135	64	Buy	72	53	42.7	28.0	3.7	3.3	9	12
Tianshui Huatian Technology	002185.SZ	Jimmy Yu	7,928	13	16	Neutral	33	27	57.0	44.8	2.8	2.7	5	6
TongFu Microelectronics Co Ltd	002156.SZ	N/A	13,526	N/A	57	N/A	50	13	45.3	40.1	5.0	4.5	10	11
Shanghai V-Test Semiconductor Tech Co Ltd	688372.SS	N/A	2,517	N/A	100	N/A	36	106	40.6	19.7	3.8	3.2	11	18
Sector Average							**58**	**47**	**39.7**	**28.0**	**4.5**	**3.9**	**13**	**17**
Tester														
Advantest	6857.T	Atsuhiro Kinoshita	191,547	43,600	41,850	Buy	80	96	38.8	53.1	16.8	31.8	70	58
Teradyne Inc	TER.O	Timothy Arcuri	67,666	500	430	Buy	134	51	45.7	30.8	16.7	12.8	43	47
Sector Average							**107**	**74**	**42.2**	**42.0**	**16.7**	**22.3**	**57**	**52**
Prober/Prober solutions														
Hermes Testing Solutions	7856.TWO	Ryan Sun	3,580	8,880	4,190	Buy	221	487	143.9	27.3	9.1	7.0	10	29
Tokyo Electron	8035.T	Atsuhiro Kinoshita	184,031	18,720	12,805	Buy	-16	71	29.7	37.1	6.5	12.8	36	44
Sector Average							**102**	**279**	**86.8**	**32.2**	**7.8**	**9.9**	**23**	**36**
Handler														
Hon.Precision, Inc.	7769.TW	Sunny Lin	33,404	10,000	5,905	Buy	90	86	45.2	24.4	14.5	10.6	36	50
Chroma ATE	2360.TW	Jerry Su	31,434	2,960	2,350	Buy	64	38	51.8	37.7	28.6	20.8	58	64
Cohu, Inc.	COHU.O	N/A	3,460	N/A	73	N/A	n.a.	94	77.0	39.6	-	-	7	16
JHT Design Co Ltd	603061.SS	N/A	4,045	N/A	312	N/A	155	47	54.8	37.3	13.0	9.9	22	25
Hangzhou Changchuan Technology	300604.SZ	Yongwei Lai	22,690	310	240	Buy	60	53	76.1	49.8	23.4	16.5	36	39
Sector Average							**92**	**63**	**61.0**	**37.8**	**19.9**	**14.4**	**32**	**39**
Test Socket														
WinWay Technology	6515.TW	Ryan Sun	6,948	8,900	6,130	Buy	119	98	60.2	30.4	22.0	14.6	44	34
Leeno Industrial Inc	058470.KQ	N/A	4,936	N/A	86,900	N/A	33	17	35.4	30.3	8.0	6.8	24	24
ISC Co Ltd	095340.KQ	N/A	3,247	N/A	205,500	N/A	70	41	47.0	33.2	7.0	5.9	16	19
Yokowo Co Ltd	6800.T	N/A	744	N/A	4,925	N/A	28	93	38.3	19.8	-	1.8	-	-
Sector Average							**62**	**62**	**45.2**	**28.4**	**12.3**	**7.3**	**28**	**26**
Load Board														
Chunghwa Precision Test Tech	6510.TWO	Ryan Sun	3,149	5,000	3,055	Buy	112	99	47.5	23.8	9.2	7.3	21	34
Probe Card														
Technoprobe SpA	TPRO.MI	Harry Blaiklock, CFA	27,100	41	37	Buy	259	18	66.9	56.5	14.6	11.6	25	23
MPI Corp	6223.TWO	N/A	17,518	N/A	5,670	N/A	97	110	87.2	41.5	30.3	19.1	38	54
FormFactor Inc	FORM.O	N/A	11,038	N/A	141	N/A	159	24	46.2	37.1	9.3	8.9	19	23
MICRONICS JAPAN CO.,LTD.	6871.T	N/A	3,906	N/A	15,410	N/A	155	28	24.8	19.4	7.1	5.6	32	36
Japan Electronic Materials Corp	6855.T	N/A	804	N/A	8,650	N/A	46	43	24.9	17.4	-	-	-	-
Sector Average							**138**	**54**	**49.6**	**32.6**	**14.1**	**10.5**	**27**	**34**

Source: LSEG, UBS estimates. Priced as of October 6 (HKT).

Valuation Method and Risk Statement

Tech investing involves risk. It is difficult for the investment community, UBS included, to project the financial results of tech companies, as their operating models are highly volatile and unpredictable, and they compete in a highly dynamic marketplace. In addition to their low predictability, valuing tech stocks can be challenging because neither traditional nor non-traditional valuation measures have provided much insight into how tech stocks trade.

We value Chroma ATE using a PE methodology.
Downside risks include weaker-than-expected demand for high-performance computing dampening its semiconductor testing business and slower-than-expected recovery in EV investments into battery capacity installations.

We value Chunghwa Precision Test, Hermes Testing and WinWay based on PE methodology.
Risks: Faster- or slower-than-expected front-end/CoWoS capacity expansion could result in CHPT, HTSI and WinWay gaining/losing probe card/board orders from major foundries and OSATs. Potential risk of competition (from either local or foreign companies) achieving technological advancements could result in these companies losing market share from end customers, major foundries, and OSATs. Better- or worse-than-expected AI growth could lead to a ramp-up or a slowdown of product orders from customers, major foundries, and OSATs to CHPT, HTSI and WinWay, affecting long-term revenue growth potential. A potential slowdown or delay of the rollout for technological advancements for technologies such as SoIC, CoPoS, and even CPO, would limit future growth potential. Rising raw material costs may directly impact their margins for equipment shipments.

We value Hon Precision based on PE multiple.
Faster- or slower-than-expected CoWoS capacity expansion could indirectly result in Hon Precision gaining or losing equipment orders from major customers; the risk of competition from either local or foreign companies achieving technological advancements could result in Hon Precision losing market share from its major customers; better- or worse-than-expected AI growth could lead to a ramp-up or a slowdown of equipment orders from customers to Hon Precision, affecting long-term revenue growth potential; a potential slowdown or delay in the rollout of technological advancements for technologies, such as MCL and CPO, would limit future equipment orders; rising raw material costs may directly impact Hon Precision's margins for equipment shipments.

