Flash | Citi Research

17 Sep 2026 06:59:13 ET | 11 pages

China PCB

Our Thoughts on CPO Impact on PCB

CITI'S TAKE

PCB names traded relatively weak today amid market concerns that CPO adoption could downgrade materials from M8/M9 to M4 as optics replace electrical SerDes traces. However, we believe the market concerns are overdone on material downgrades while underestimating PCB dollar-content resilience. Our check with PCB makers indicates CPO sample boards still utilize **M8-class CCL with ~40–50 layers**, showing no notable downgrade so far. While CPO structurally shortens electrical SerDes channels, the overall impact is less severe than feared: other high-speed interfaces, thick boards, vias, and connectors may still demand M6–M8 materials. Crucially, a lower material downgrade does not equal lower PCB value content. **Rising PDN complexity, power/ground requirements, package breakout density, and manufacturing difficulty** will continue supporting high-end PCB value-add. Among our PCB coverage, we prefer **WUS** on board-based switch makers exposure and high-quality execution and believe it should benefit from high-speed SerDes and even CPO switch migration.

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Market concern vs. current reality. Recent market discussions suggest that CPO could significantly reduce PCB/CCL specifications. Under the conventional architecture, 224G SerDes signals need to travel relatively long distances across the system PCB, requiring M8/M9-class ultra-low-loss CCL. With CPO moving the optical engine closer to the switch ASIC, these high-speed electrical channels can be substantially shortened, leading to concerns that system-board CCL could eventually fall to M4 and that PCB value content could decline accordingly. However, our check with PCB makers suggest that **current CPO sample boards continue to use M8-class materials and remain at ~40–50 layers**, implying no meaningful downgrade at this stage. We believe M8 remains necessary partly because CPO only shortens the most demanding ASIC-to-optical-engine SerDes channels rather than eliminating all high-speed electrical connectivity on the board. In addition, CPO remains at the sampling/early adoption stage, where customers are more likely to retain proven high-speed stack-ups and sufficient SI margin before pursuing subsequent material cost-down.

Material downgrade risk is probable, but likely more gradual/less than the market expects... Under the conventional architecture, each increase in SerDes speed raises PCB insertion-loss requirements, driving material migration from M7 toward M8/M9 and supporting material/PCB ASP expansion. By moving the optical engine next to the ASIC, CPO removes or substantially shortens the most challenging 224G electrical channels, reducing the need for the highest-grade low-loss materials on the system board. However, we do not expect a migration to an M4-only solution, as

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such a transition would require most high-speed electrical traffic to be removed from the system PCB and the remaining channels to operate within a sufficiently relaxed loss budget, which could be challenging for large, high-layer-count boards with complex routing, vias and connectors. Importantly, our checks with PCB makers suggest that current CPO samples still use M8-class materials, indicating that designers continue to prioritize SI margin and proven stack-ups at this stage. We therefore expect material optimization to be gradual as CPO designs mature, potentially through selective material downgrade and hybrid stack-ups, rather than a wholesale transition from M8 to M4.

...and does not necessarily mean lower PCB dollar content. PCB makers indicated that the CPO-related boards it currently sees remain at roughly **40–50 layers**, and it does not expect CPO to materially reduce PCB value content. We think the underlying logic is reasonable: CPO reduces the Signal Integrity burden associated with long-reach high-speed SerDes, but next-generation switch ASICs continue to increase in power and I/O density, driving greater PDN complexity, power/ground layer requirements, package breakout density and overall routing complexity. As a result, fewer high-speed SerDes layers do not necessarily translate into lower total layer counts. Moreover, PCB manufacturing value-add is driven not only by CCL grade, but also by layer count, lamination cycles, drilling/via density, large-board manufacturing complexity and yield requirements.

WUS Printed Circuit

(002463.SZ; Rmb123.48; 1; 17 Sep 26; 15:00)

Valuation

We apply 25x 2027E P/E to derive our target price of Rmb161.0 for WUS, which we believe is justified by an 81% 2026-28E earnings CAGR driven by: 1) robust growth backed by GenAI-related PCB demand during 2026-2028E; 2) potential ASP/GM improvement thanks to a favorable product mix; and 3) strong execution and delivery capabilities to help sustain a robust GM.

Risks

Key downside risks that could impede the stock from reaching our TP include: (1) less-than-expected share allocation in GenAI-related PCB, (2) pricing and competition pressure in automotive supply chain; (3) CSP capex reduction and weak economy lowering demand; (4) increasing materials costs; and (5) US-China geopolitical risk.

