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Greater China Semi

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EQUITY: TECHNOLOGY

Equipment supply, photonics, and thermal

Our key takeaways from SEMICON Taiwan 2026

Key observations from SEMICON Taiwan 2026: Extended equipment lead time vs. the urgency to add more supplies; photonic equipment showcase; thermal management solution discussion

We attended SEMICON Taiwan 2026, which was held from 31 August to 4 September. While AI/HPC continue to be the primarily driving force of technology evolutions in semiconductor fabrication and assembly, an incremental change we observed at the event was an increase in the number of companies demonstrating their solutions for photonic testing and assembly.

We profile our findings from the event below:

1. IC substrate supply additions could be constrained by an extending equipment lead time. Based on our findings at the event, the lead time of Nikko-Materials' (unlisted; a subsidiary of Eternal Precision Mechanics [7795 TT, Not rated]) ABF vacuum laminator has risen to two years, vs. six months in April/May. Nikko-Materials' laminators have a near monopolistic position in high-end ABF substrates, but its tool capacity expansion appears to be slower than existing substrate makers' expansion.
2. We noted before that Toray Engineering's (unlisted; a subsidiary of Toray Industries [3402 JP, Neutral]) die bonders are the critical tools for bridge die embedding at Intel's (INTC US, Not rated) EMIB-T substrate partners (*report*). We notice the lead time of the die bonder is around 12 months, and the move-in schedule is managed by Intel with planned shipments through end-2027E. We think Google's (GOOG US, Not rated) potential reliance on Intel's EMIB-T for the next-generation TPU v9 (partnering with MediaTek [2454 TT, Buy]) could be a critical litmus test for Intel's advanced packaging capabilities. On top of the bridge die bonder lead time, coefficient of thermal expansion (CTE) mismatch between silicon and organic films, and build-up layer cavity precision appear to be two major manufacturing challenges.
3. An issue in discussion is the low throughput of ficonTEC's (unlisted; a subsidiary of RoboTechnik [300757 CH, Not rated]) double-sided wafer test in co-packaged optics (CPO) test insertion 2, and whether TSMC (2330 TT, Buy) and end-customers would consider bypassing the testing. While skipping insertion 2 might improve the overall cycle time, we note that certain test items cannot not be covered by subsequent test insertions, and insertion 2 also plays an important role to gate foundry yield and identify the supply chain accountability, as the rest of CPO processes take place in the venue of OSATs (i.e. TSMC is only involved in optical engine [OE] production). As such, we reason that the supply chain dynamics and process flows remain fluid, and that there is no uniform standard or firm conclusion how the entire process would shape up.
4. In our *Advanced Semi Testing Anchor Report*, we noted that the CPO test insertion 3 might involve sheer die-level OE test, and package-level test after receptacle assembly/structural reinforcements. Based on our observation at the event, package-level test could be the one chosen by Mellanox (unlisted; under nVidia [NVDA US, Not rated]) for its initial Insertion 3 ramping, but the die-level test appears to be an option considered by many vendors. Chroma (2360 TT, Buy) and ficonTEC both have solutions for the package-level test for OE; MPI (6223 TT, Buy) has a probing solution for the die-level test.
5. While several companies demonstrated optical coupling tools (for receptacles, fiber array units [FAUs], etc.), key parameters of debate are throughputs and precision,

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notably considering the active alignment required. Our conversations during the exhibition suggest there could be possibility of two equipment vendors at least for receptacle coupling with OEs. Meanwhile, we flagged before that Largan's (3008 TT, Buy) high-precision assembly and full automation capability are two of the advantages when tapping into CPO component production (*report* and *report*), which were acknowledged by other equipment makers during our booth visits.

6. While burn-in test (BIT) is an optical procedure in semiconductor backend, the surge in chip thermal design power (TDP) and rising need for reliability (notably for external chip sales) of AI/HPC steer the necessity for BIT and could therefore foster the demand for mass production burn-in ovens. High-power burn-in capability and automation are two critical aspects in our view, and vendors that have gained solid foothold include KYEC (2449 TT, Buy; proprietary ovens) and AEM (AEM SP, Not rated). The addition of BIT could also present potential opportunities to BIT interface vendors such as CHPT (6510 TT, Buy) and WinWay (6515 TT, Buy).
7. We observed an increased focus on thermal solutions in forum speeches, as AI/HPC chips are driving more stringent thermal management challenges. Lidded AI chips are looking for better structural supports, CTE matching, and thermal spreading, and two-/multiple-piece lids are currently on the radar of chip designers. Aside from more advanced architectures such as vapor chamber lid (VCL) and microchannel lid (MCL), future lid-/ring-type designs will also involve in material innovations contemplating CTE, thermal conductivity (for lid)/Young's modulus (for ring), and manufacturability, and we notice copper-diamond and thermadite (by Coherent [COHR US, Not rated]) are potentially materials under investigation. We had an extensive discussion about heat dissipation technologies in *our October 2025 Asia AI Thermal Anchor Report*.

Stocks for action: Buy key AI enablers; remain positive on OSAT spending cycle beneficiaries

We reiterate our Buy rating on **TSMC (2330 TT)**, for its AI-enabler position and strengthened growth outlook, and on **Unimicron (3037 TT),** which is benefiting from more favorable pricing conditions amid supply bottleneck and technological advancements (EMIB-T with manageable risk-reward, and large reticle-size 2.5D). Advanced logic complexity and reliability requirements should continue to spur OSAT spendings, and we have Buy ratings on advanced semiconductor testing supply chain names – **Hon Precision (7769 TT)**, **Chroma (2360 TT)**, **MPI (6223 TT)**, **WinWay (6515 TT)**, **ASE (3711 TT)**, and **KYEC (2449 TT)**.

Appendix A-1

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