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BERNSTEIN
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EU Semiconductors

ASML: High-NA EUV Primer - The shrinking never stops



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Logic and DRAM process nodes continue to shrink, and lithography is at the center stage driving that shrinking. High NA (HNA) is the next tool to enable further shrinking. More than a decade after HNA R&D started, this system is now finally approaching HVM adoption, possibly from 2027. This primer explains the technology, drivers for adoption, and It is also a companion to our previous HNA report (ASML: HNA cost deep dive) which discusses HNA cost vs. LNA EUV and explains why DRAM is likely the first to adopt, but eventually it's more economical for all players to adopt HNA. The drivers for HNA adoption are clear: **advanced logic and DRAM scaling will continue, and HNA will win over time given both cost and performance merits.**

HNA has clear performance benefits. Using a new 0.55 NA anamorphic optical system, keeping the same 13.5nm EUV wavelength but improving resolution from roughly 13nm to 8nm and increasing imaging contrast, the benefit is clear: **smaller features, tighter pattern control, lower dose, fewer masks, simpler process flows and potentially better yield.** But the architecture also creates challenges. The anamorphic design cuts the exposure field roughly in half, which hurts throughput and creates stitching requirements for large logic die. ASML partially offsets this with faster wafer and reticle stages, lower dose and roadmap throughput improvements. Notably, HNA economics must be judged at the full patterning flow level, not scanner WPH alone.

HNA's initial cost advantage over LNA depends on stitching, but the gap widens over time. Our cost analysis suggests HNA adoption is likely to be focused on layers where LNA multi-patterning becomes too complex and costly. HNA exposure cost is still high today, mainly because availability and throughput are still maturing, but the cost curve improves materially as uptime moves toward LNA levels and productivity increases. **In logic,** where stitching is required, 1x HNA SE is already cheaper than 3x LNA EUV exposures, but remains more expensive than 2x LNA double patterning. **In DRAM,** where stitching is not required, HNA is already cheaper than LNA double patterning, with a larger advantage against more complex multi-patterning schemes.

For this reason, we expect DRAM to see broader HNA adoption first, led by Samsung and SK hynix around 2027 (D1d), while logic adoption is likely to expand more gradually between 2028 and 2030. Intel has already demonstrated HNA readiness in HVM with 18A and will likely expand usage at A14, while Samsung and TSMC appear more likely to adopt HNA at A10-class nodes around 2030 as tool productivity improves further. **Importantly, slower HNA adoption does not weaken its economic case** and could even benefit ASML near term by extending demand for high-margin LNA tools before customers consolidate layers onto fewer HNA systems.

The strategic implication is higher litho intensity. HNA lowers total patterning cost by reducing process complexity, but shifts more value into litho because one HNA exposure can replace multiple LNA and non litho steps. In logic, HNA enables critical local interconnect, via and metal layers to move from LNA MP to HNA SE, with around 20% to 35% cost benefit. In DRAM, the case is even cleaner: HNA can replace complex contact hole multi patterning, reduce dose, improve LCDU. **We reiterate ASML Outperform for higher capex and litho intensity for both DRAM and Logic.**

See the Disclosure Appendix of this report for required disclosures, analyst certifications and other important information. Alternatively, visit our Global Research Disclosure Website.

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BERNSTEIN TICKER TABLE

			1 Sep 2026		TTM	Reported EPS				Reported P/E (x)	
			Closing	Price	Rel.						
Ticker	Rating	Cur	Price	Target	Perf.	Cur	2025A	2026E	2027E	2025A	2026E	2027E
ASML.NA (ASML)	O	EUR	1,435.40	2,500.00	107.6%	EUR	24.72	38.91	53.56	58.1	36.9	26.8
ASML (ASML)	O	USD	1,696.01	2,859.00	104.3%	USD	27.95	44.01	60.58	52.2	33.2	24.1
EDME			1,614.14									
SPX			7,686.14									

O - Outperform, M - Market-Perform, U - Underperform, NR - Not Rated, CS - Coverage Suspended

Source: Bloomberg, Bernstein estimates and analysis.

INVESTMENT IMPLICATIONS

We rate ASML Outperform, PT = €2,500 and top pick.

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DETAILS

Our ASML Model and Industry models can be downloaded here (ASML.NA / ASML Holding NV; EUV Model; DUV Model).

SHRINKING CONTINUES IN BOTH LOGIC AND DRAM

Despite recurring concerns that Moore's Law is slowing, both logic and DRAM roadmaps continue to point toward meaningful lateral scaling over the next decade. **Continued scaling remains one of the semiconductor industry's most important objectives because it enables higher performance, lower power consumption, greater functionality and lower cost per transistor or bit.** The rapid expansion of AI, cloud computing, high-performance computing and advanced mobile devices continues to drive demand for more compute and memory density. While innovations such as GAA transistors, advanced packaging and HBM architectures are important, they complement rather than replace lithography-driven scaling. Ultimately, delivering more transistors, larger caches and higher memory capacity within practical power and cost budgets still requires smaller features and tighter pitches.

In logic, industry roadmaps from imec and leading foundries indicate that metal pitch is expected to decline from roughly **40nm at N7 in 2018 to ~21nm at A14 around 2027**, and potentially into the **14-10nm range beyond A2**. As pitches shrink, CPUs, GPUs and AI accelerators can pack more logic into a given area, improve routing efficiency and increase performance per watt. However, patterning these layers becomes progressively more difficult. At advanced nodes, LNA EUV increasingly relies on double and triple patterning to maintain the required resolution and edge placement accuracy, resulting in more masks, higher

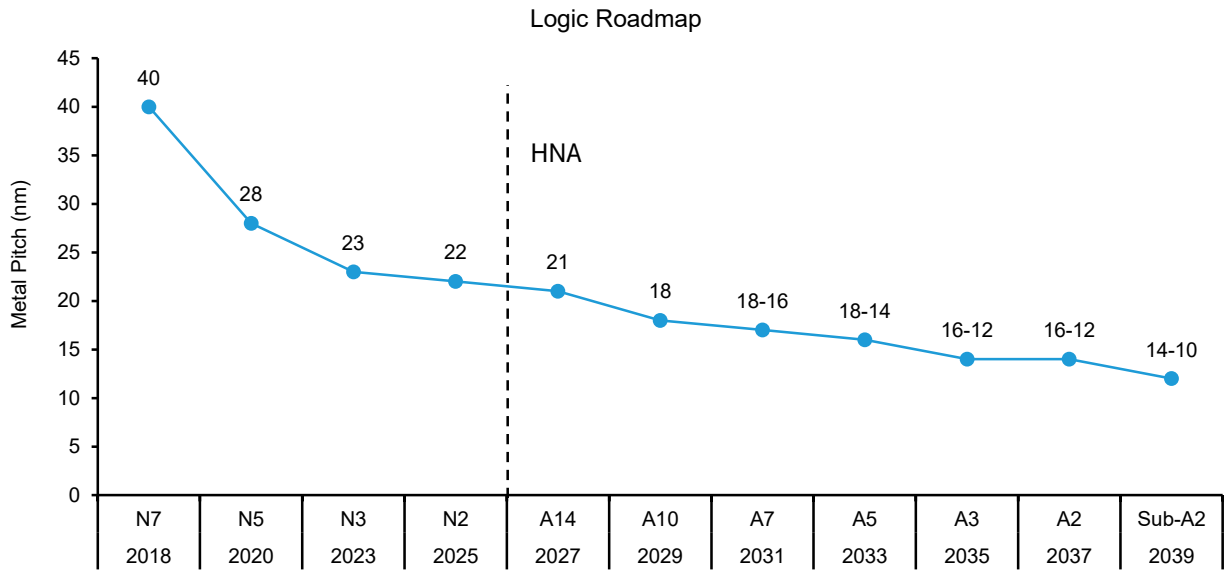
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cost, longer cycle times and greater process complexity. This is why future logic scaling becomes increasingly dependent on higher-resolution lithography (Exhibit 1).

The same trend is evident in DRAM. Memory demand continues to grow rapidly, particularly from AI servers and HBM, creating a constant need for higher bit density and lower cost per bit. Based on industry roadmaps, DRAM feature size (F) is expected to decline from roughly **17-18nm at 1Y to around 10nm at 1d**, before moving toward the **7-8nm range at future 0x generations**. Smaller features allow manufacturers to store more bits on each wafer, improving both density and economics. However, as contact holes and critical memory features approach 10nm, conventional LNA EUV increasingly requires complex multi-patterning schemes, raising manufacturing cost and reducing productivity (Exhibit 2).

Notably, device architecture innovations such as GAA, CFET and advanced DRAM cell designs remain important, but they ultimately require continued improvements in patterning capability. For this reason, we view continued lithography advancement as a prerequisite for future node migration. The combination of ongoing logic metal pitch shrink and DRAM feature-size reduction supports our view that demand for EUV will continue to increase through the end of the decade. As a result, HNA should be viewed not as a discretionary technology upgrade, but as the next logical step in extending semiconductor scaling once LNA multi-patterning becomes too complex, costly and patterning-limited.

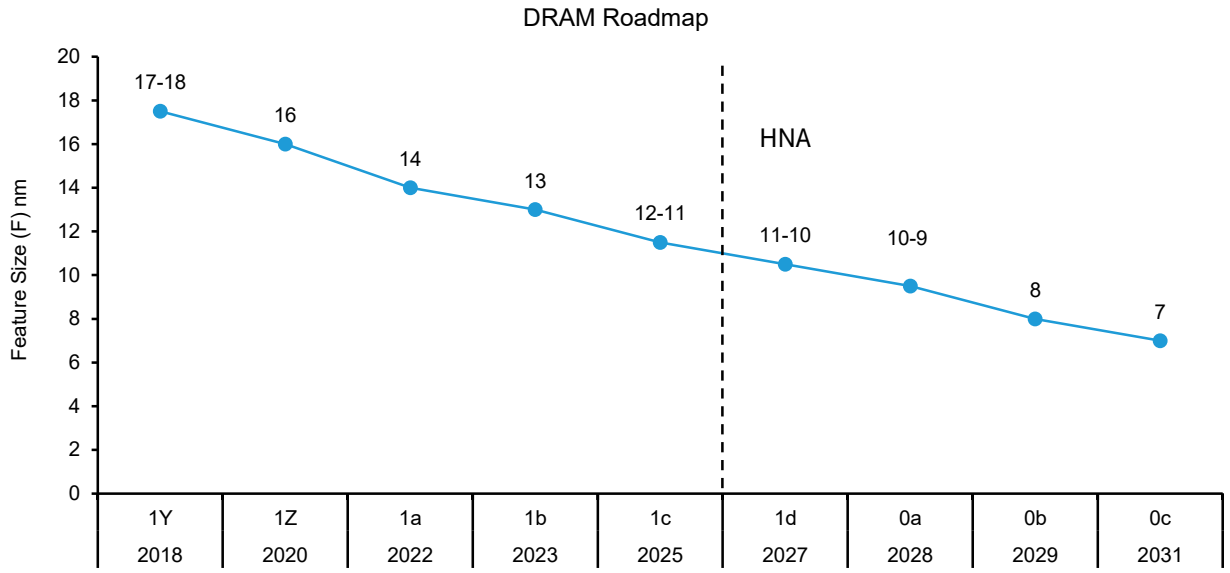
EXHIBIT 1: **Logic metal pitch will continue to shrink. Although Intel has already adopted HNA with 18A, we estimate broader logic adoption will occur around A14 in the 2027-2030 timeframe, when metal pitch is expected to decline to approximately 21-18nm.**



Source: Company reports, Imec, Bernstein analysis and estimates

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EXHIBIT 2: **Similarly, DRAM feature size is expected to continue shrinking, entering the sub-10nm era with the 0x generations. We believe DRAM manufacturers could begin adopting HNA at the 1d node around 2027-2028, when the minimum feature size is expected to reach 10nm.**



Source: TEL, ASM International, Bernstein analysis

LITHOGRAPHY: THE CRITICAL STEP BEHIND CHIP SCALING

Before diving deeper into High-NA, it is important to understand what lithography is, how it works, and how it has evolved over time.

WHAT IS LITHOGRAPHY?

The word "lithography" originates from Ancient Greek and refers to the process of printing from a stone or metal plate with pre-drawn images onto a blank sheet of paper. In the semiconductor industry, the concept of lithography is similar — the process of using light to transfer the patterns from a "photomask" onto a light-sensitive chemical “photoresist” coated on the wafer.

The fabrication of semiconductor chips requires a variety of process steps, and lithography is arguably the most important one as it transfers the tiny patterns that define each chip layer onto the wafer. Because lithography determines the smallest features that can be printed, it directly controls how densely transistors and memory cells can be packed. **By printing smaller features, lithography enables later scaling, allowing more transistors to fit in the same area and improving chip performance, power efficiency, and cost.**

LITHO PROCESS

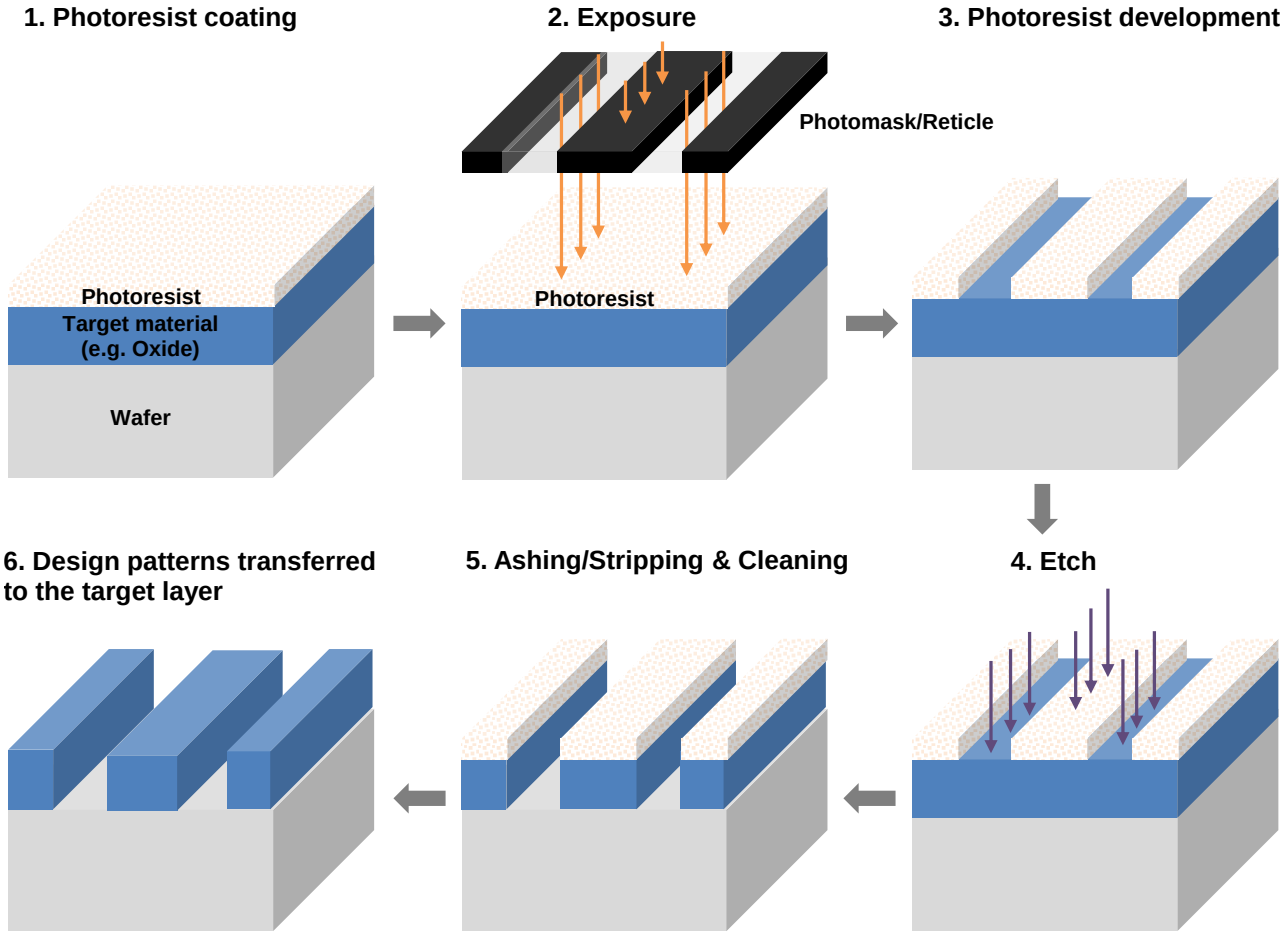
In a lithography process (Exhibit 3), the Litho equipment first exposes the wafer covered with photoresist to light through a photomask, sometimes called a mask or reticle. A photomask is a piece of fused silica (quartz). It comes in different sizes, but the 6" photomask is most commonly used. Excluding the surrounding area on the side for other purposes (e.g., handling and alignment), a 6" photomask will have an area of 104mm x132mm to contain the pattern designed by circuit designers and, typically, 4x of the actual pattern in length (i.e., 16x in area). Depending on the pattern on the photomask, some parts are opaque and block light from passing through and other parts allow light to transmit through.

A series of lenses focuses the transmitted light and shrinks the pattern to 1/16, transferring the pattern at the correct size onto the wafer surface that is coated with photoresist. Only selected areas of photoresist are exposed to light, and the chemical change caused by the exposure to light allows only the designated areas of the photoresist to be washed away by a special solution — a "photoresist developer." Thus, the design patterns on the photomask are transferred onto the photoresist, which acts as a protecting layer in the subsequent process steps. This printing-like method enables semiconductor manufacturers to fabricate a high-volume of semiconductor chips with very fine and complex structures in a precise and efficient way. The capability of the lithography equipment usually determines the smallest lateral size of the pattern that can be created and,

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therefore, plays a critical role in the advancement of technology in the semiconductor industry. This also explains why many believe lithography technology is pivotal to the long-term viability of Moore's Law.

EXHIBIT 3: **Lithography is the process of using light to transfer patterns from a photomask onto a light-sensitive chemical "photoresist" coated on wafers**



Source: Bernstein analysis

LITHO INTENSITY ON THE RISE AS SHRINKING CONTINUES

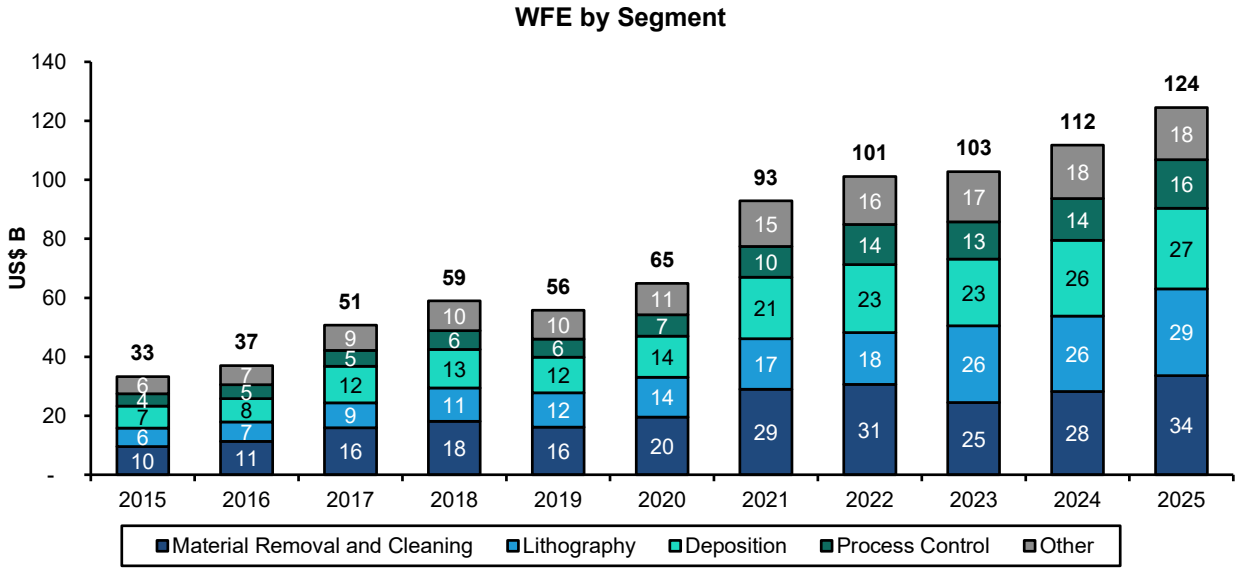
The industry also often looks at "litho intensity", defined as lithography equipment spend as a % of total WFE. In simple terms, it measures how much of every dollar spent on front-end equipment is allocated to lithography tools. Historically, litho intensity has fluctuated depending on the mix of logic, memory, and mature-node capacity additions, but over the past decade it has typically remained in the high-teens to low-twenties range. **Since 2023, however, lithography spend has increased meaningfully to around 23–25% of WFE. This step-up has been driven primarily by the accelerating ramp of advanced logic and DRAM, both of which require significantly more advanced patterning steps** (Exhibit 4, Exhibit 5).

In advanced logic, the transition to leading-edge nodes has increased the number of critical layers exposed using EUV lithography. EUV enables finer patterning with fewer multi-patterning steps, but EUV scanners are also significantly more expensive than traditional DUV tools, raising the lithography share of total fab spend. In DRAM, litho intensity has also increased as manufacturers adopted EUV at 1a-class nodes and expanded its use in sub-1a generations to improve pattern fidelity and reduce process complexity, and support higher-density memory architectures. The growth of AI and high-performance computing has further strengthened demand for advanced logic and high-bandwidth memory (HBM), reinforcing this mix shift toward lithography-heavy capacity. Another important factor is China-related demand. Following tightening US export restrictions on the shipment of the most advanced lithography systems to China, Chinese fabs increased orders for eligible DUV tools.

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ASML is the primary beneficiary of this structural increase in litho intensity. The company dominates the lithography equipment market, with over 90% share in overall lithography and a monopoly position in EUV systems, where ASML is the only supplier. This unique position has allowed ASML to become the world's largest semiconductor equipment supplier by revenue despite specializing only in lithography and having little presence in the rest of the WFE market. ASML's share of total WFE increased from roughly 16% in 2022 to around 22% in 2025, reflecting both higher litho intensity and ASML's unrivalled position in EUV and advanced DUV tools (Exhibit 6).

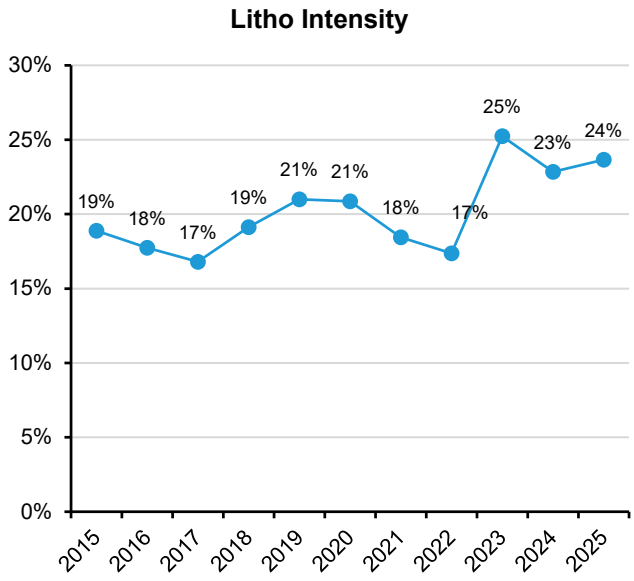
EXHIBIT 4: **Lithography was the second largest WFE segment in 2025, reaching USD 29bn. Over the last decade, it was the fastest-growing WFE category, expanding at a 17% CAGR versus 14% for the broader WFE.**



Source: Gartner, Bernstein analysis

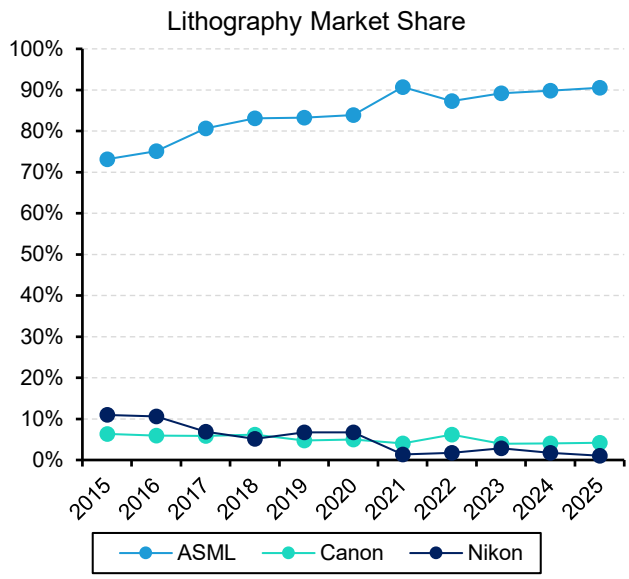
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EXHIBIT 5: **Litho intensity has structurally reset above historical levels, rising from 17% in 2022 to 25% in 2023, before stabilising at 23% to 24% as EUV adoption increases in logic and DRAM.**



Source: Gartner, Bernstein analysis

EXHIBIT 6: **ASML maintained over 90% lithography market share in 2025, reinforcing its dominant position as the sole EUV supplier and key beneficiary of rising lithography intensity across WFE.**



Source: Gartner, Bernstein analysis

EVOLUTION OF LITHOGRAPHY

To understand the evolution of lithography, we first need to understand some of the principles of how these systems work. **The minimum feature size that a stepper or scanner can print is governed by Rayleigh's Equation:**

$$CD = k_1 \times \lambda / NA$$

where CD is the minimum feature size (also called the critical dimension), λ is the wavelength of the light source, NA is the numerical aperture, and k_1 is a coefficient that encapsulates process-related factors (Exhibit 7). Better resolution (smaller CD) can be achieved by using either a light source with a shorter wavelength, optics with a higher numerical aperture, or lower k_1 through better process control (e.g., holistic lithography that integrates computational lithography, wafer printing, and process control).

Lithography systems over the last 40+ years have used ultraviolet light, with the i-line and g-line systems of the 1980s using wavelengths of >300nm, followed by KrF systems using a wavelength of 248nm in the 1990s. And in the early 2000s, ArF systems moved to a wavelength of 193nm (Exhibit 8).

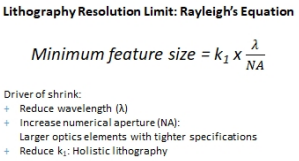
Until 2018, the state-of-the-art scanners used in the mass production of semiconductors were 193nm "immersion" systems. They use deep ultraviolet (DUV) light with 193nm wavelength and replace the usual air gap between the final lens and the wafer surface with a liquid medium. The liquid medium has a refractive index greater than one, which reduces the effective wavelength. **DUV tools, ArF i and older models, will remain the industry's main workhorse across both mature and advanced nodes.** In mature nodes, DUV offers the best cost-performance balance, with higher throughput than EUV tools and strong demand from analog, power and other mature applications. In advanced logic and DRAM, DUV remains essential for non-critical layers alongside EUV. Rather than being cannibalised, DUV demand should remain resilient as overall wafer complexity and capacity continue to grow.

As the semiconductor industry pursued smaller and smaller transistors, 193nm immersion lithography equipment reached its limit. By using light of narrower wavelength to reduce critical dimension, EUV lithography succeeded 193nm "immersion" and is now the most advanced lithography technology with a wavelength of 13.5nm (Exhibit 9).

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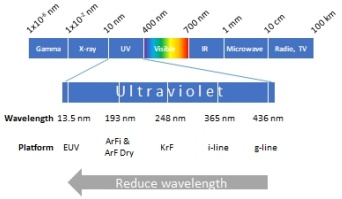
Lowering k1 is another way to improve lithography resolution, alongside shorter wavelength and higher NA. A lower k1 depends on multiple factors: scanner performance, source wavelength control, photoresist, photomasks, OPC and other resolution enhancement techniques. Multi patterning can also push effective k1 lower, including below the traditional 0.25 physical limit, but at the cost of more exposures, lower throughput, higher process complexity and potentially lower yield. For EUV, reducing k1 is especially important because EUV introduces additional process control challenges versus DUV. The industry has historically reduced k1 over time, but doing so becomes harder as dimensions shrink.

EXHIBIT 7: **Making wavelengths shorter is an important means to enhance the precision of lithography tools...**



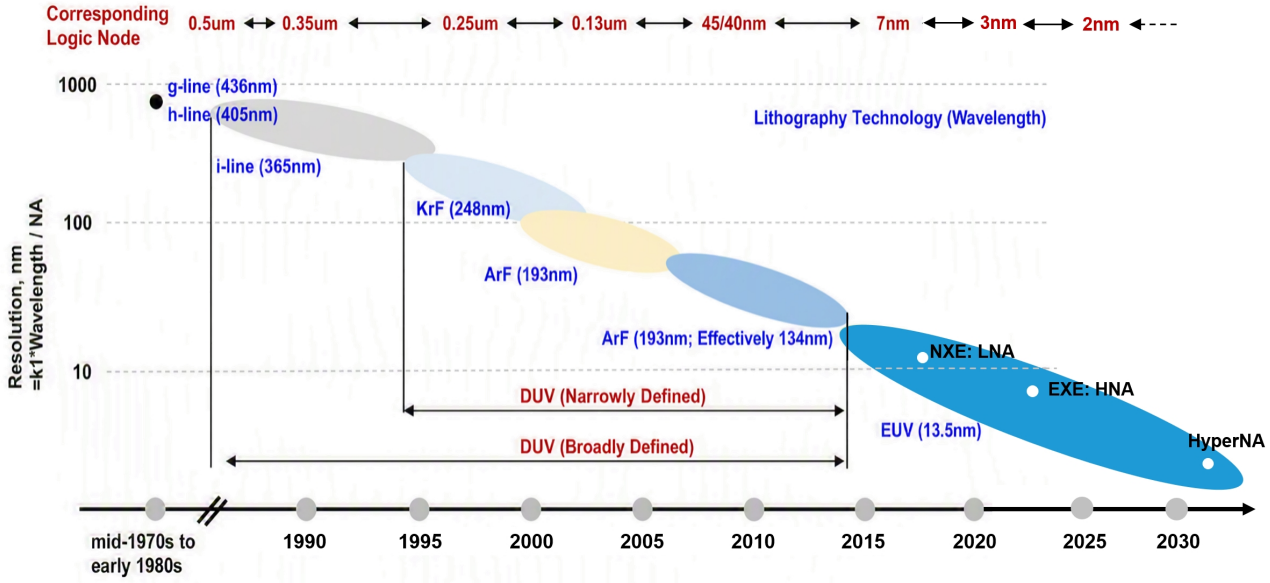
Source: Bernstein analysis

EXHIBIT 8: **... and the industry has transitioned from g-line in the early 1980s to the current most advanced EUV systems**



Source: Bernstein analysis

EXHIBIT 9: **Lithography resolution has improved from i-line to EUV as wavelength and numerical aperture advances enabled shrinking node sizes, supporting continued semiconductor scaling toward sub-10nm patterning.**



Source: ASML, Bernstein analysis

EUV DELIVERED A TECHNOLOGY BREAKTHROUGH IN SEMICONDUCTOR MANUFACTURING

EUV lithography uses extreme UV light with 13.5nm wavelength to print tiny features onto a wafer. With a shorter wavelength, EUV is able to achieve much higher resolution than DUV tools, allowing chipmakers to meet the patterning requirements of leading-edge nodes. ASML, the sole supplier of EUV systems, began delivering these tools to customers as early as 2010, with TSMC receiving one of the first systems. However, EUV did not enter high-volume manufacturing (HVM) until 2018–2019. The next major advancement in lithography equipment was High-NA EUV, with the first system shipped in Q4 2023. These tools feature a numerical aperture (NA) of 0.55 and are capable of printing features with critical dimensions of ~8 nm. Looking further ahead, ASML is expected to develop a next-generation Hyper-NA platform over the coming decade, increasing the numerical aperture to 0.75.

EUV required a fundamental redesign of lithography tools versus DUV. The first challenge is that 13.5nm EUV light is absorbed by air and cannot pass through conventional lenses. The solution was to operate the system in vacuum and

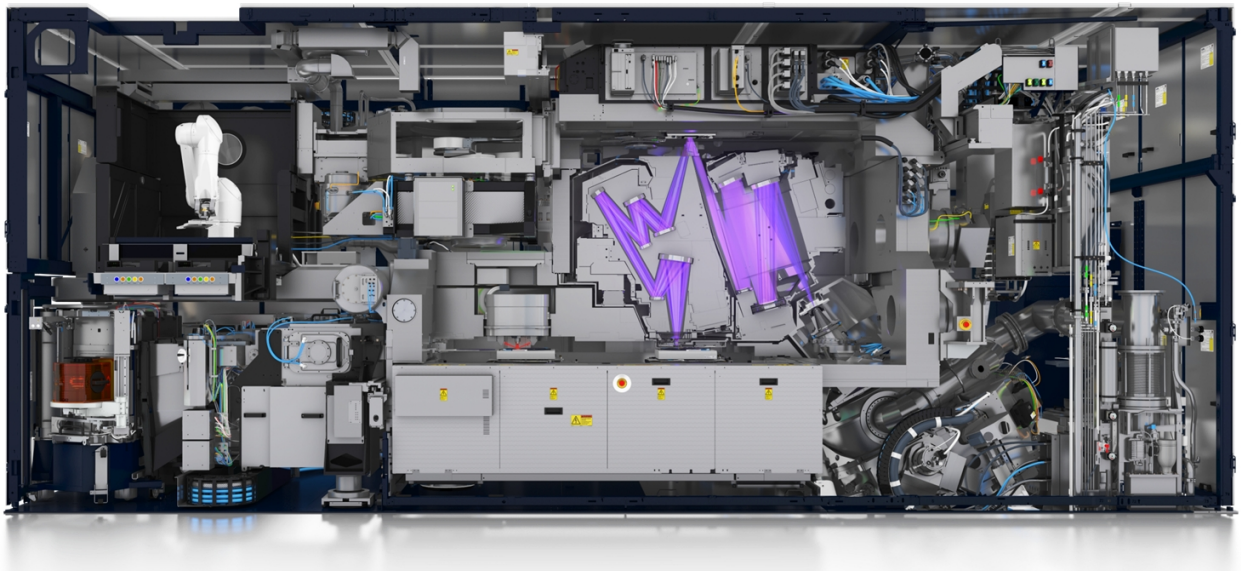
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replace DUV-style refractive lenses with a chain of highly precise reflective mirrors. This creates a second-order challenge, as every reflection absorbs part of the light, making mirror quality, alignment and optical efficiency critical to throughput. ZEISS is ASML's strategic optics partner and supplies the mirrors used in EUV systems with optical components positioned with nanometre-level precision. This becomes even more important in High-NA EUV, where larger and more precise optics are required to increase numerical aperture from 0.33 to 0.55 and support finer resolution. ASML reinforced this partnership in 2016 by acquiring a 24.9% stake in Carl Zeiss SMT for €1bn.

The second major challenge is generating enough EUV light for high-volume manufacturing. Unlike DUV, EUV light is not generated directly by a conventional laser. Instead, a high-power CO_2 laser fires at microscopic tin droplets inside the source vessel, turning the tin into plasma that emits 13.5nm EUV radiation. This light-source problem was one of the key bottlenecks that delayed EUV adoption for many years. ASML acquired Cymer in 2013 specifically to accelerate EUV source development, while TRUMPF (private) supplies the high-power CO_2 laser amplifier used in the EUV light-generation process. The EUV system uses 50,000 tin droplets per second to generate EUV light.

In short, the shift to EUV was not just a move to a shorter wavelength. It required a new architecture based on vacuum operation, mirror-based optics, laser-produced plasma light sources and much tighter system control (Exhibit 10, (Exhibit 11).

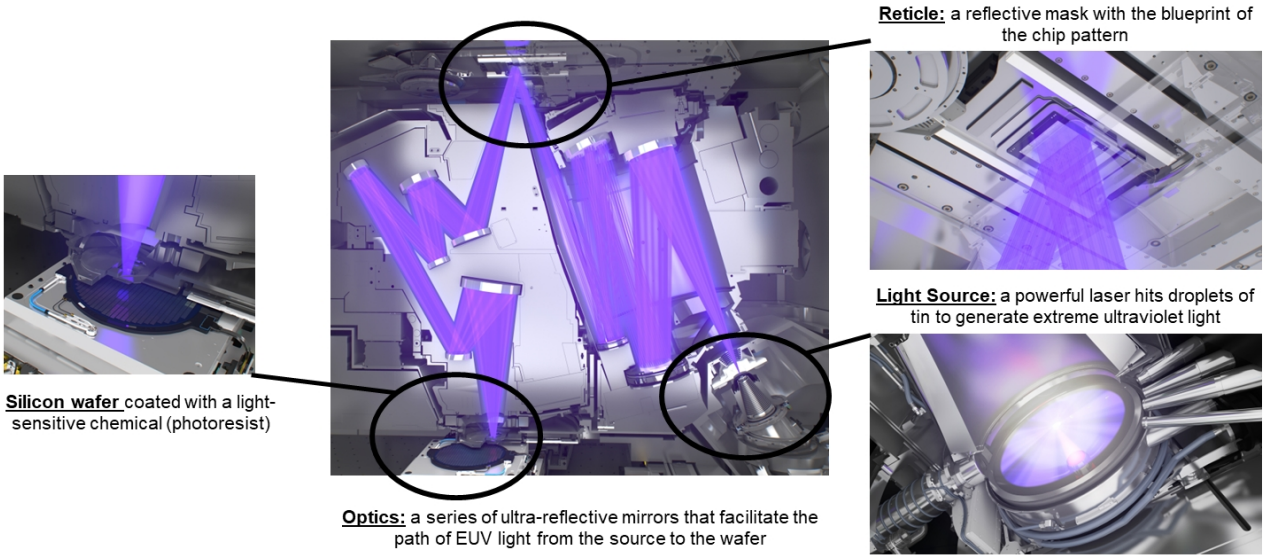
EXHIBIT 10: **ASML NXE EUV systems enable manufacturing at the 7nm node and beyond.**



Source: ASML

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EXHIBIT 11: **EUV is arguably the most complex piece of equipment in the history of the semiconductor industry**



Source: ASML, Bernstein analysis

ASML CONTINUES TO IMPROVE EUV SYSTEMS

With the successful commercialization of EUV in 2018-19, EUV tools are now extensively used in advanced logic manufacturing starting at the 7nm node, with EUV intensity increasing significantly at subsequent nodes. EUV is also being gradually adopted in DRAM, beginning with the 1a node, and here too the number of EUV layers increases considerably at the most advanced nodes, including 1b, 1c, and 1d in 2027. **The key reason behind this broad adoption is that ASML has consistently improved the technology year after year, supporting higher ASPs for EUV systems. Most important improvements are:**

1. **Throughput:** EUV throughput has improved from 130/140 WPH in 2020 to 220 WPH with the NXE:3600D in 2024. During its Q1 2026 results, ASML disclosed an updated EUV product roadmap showing significantly higher throughput for next LNA systems. The company now expects the NXE:3800F to reach 260 WPH, the NXE:4200G to increase further to 300 WPH, and the NXE:4200H, planned for release after 2030, to achieve 330 WPH. This substantial increase in throughput is primarily driven by higher source power, which is expected to rise from the current 500 to 600 watts range to 740 watts and ultimately to 1,000 watts by the end of the decade. Every incremental watt of source power directly improves throughput and lowers the cost per printed layer. Historically, throughput and ASP have shown a very strong correlation (Exhibit 12).

2. **Accuracy:** Overlay, which measures how accurately a newly patterned layer is aligned with patterns that were previously printed on the wafer, has improved from above 1nm to 0.9nm with the NXE:3800E and is expected to reach 0.7nm by the end of the decade. This improvement is particularly important for increasing yield, especially at future leading edge nodes such as A10 and sub-1nm.

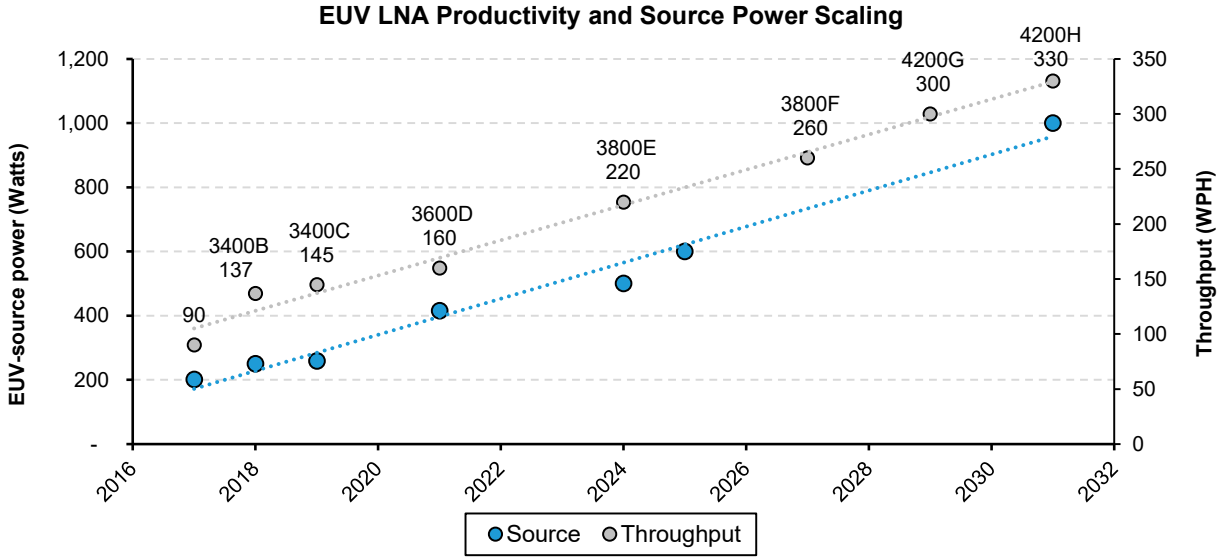
3. **Availability:** All semiconductor equipment requires maintenance, whether scheduled or unscheduled when tools encounter operational issues. In 2020, EUV uptime was in the low 80% range. Today, EUV systems are achieving uptime levels close to 95%.

4. **EUV pellicle:** A pellicle is an ultra-thin membrane positioned above the EUV reticle to prevent particles from landing directly on the mask and being repeatedly printed as wafer defects. The key trade-off is that while the pellicle improves yield, it also absorbs some EUV light, requiring longer exposure times and reducing scanner throughput. EUV pellicles are technically challenging because they must transmit 13.5nm EUV light, which is absorbed by most materials, while also withstanding high temperatures in a vacuum environment. ASML pioneered EUV pellicle technology and later industrialized the supply chain through Mitsui Chemicals (not covered). Mitsui began commercial production of EUV pellicles in 2021 under an ASML license. Since then, development has focused on improving transmittance, thermal durability, and compatibility with higher

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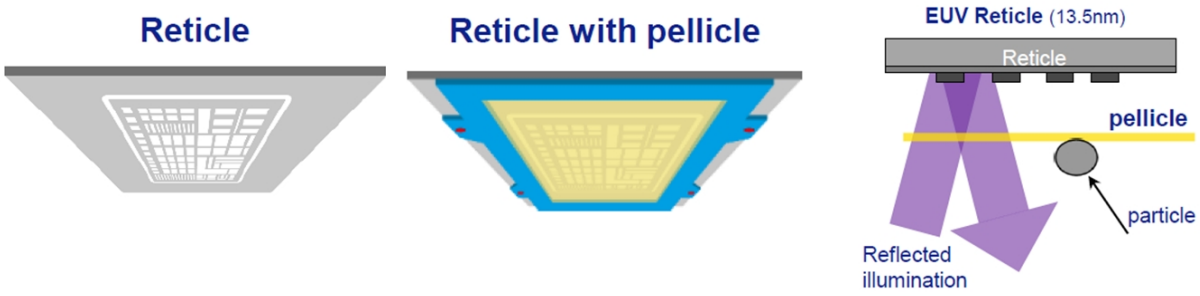
EUV source power. The next step is carbon nanotube, or CNT, pellicles. Mitsui and IMEC are working to commercialize membranes with at least 94% EUV transmittance, low reflectance, and sufficient durability for future high power EUV systems operating above 600W and potentially beyond 1kW. This is particularly relevant for next generation EUV and High NA tools, where higher source power and tighter patterning requirements make pellicle performance increasingly critical (Exhibit 13).

EXHIBIT 12: **ASML EUV product roadmap shows significantly higher throughput in next-generation systems. They now expect the 3800F to reach 260 WPH, the 4200G to further increase to 300 WPH, and the 4200H version, planned for release after 2030, to reach 330 WPH.**



Source: Company reports, Bernstein analysis

EXHIBIT 13: **Pellicle is a thin membrane that covers a photomask to keep particles from falling on the photomask; it improves production yield, but also absorbs light, thereby reducing EUV system throughput**



Source: ASML

HNA EUV: THE NEXT SCALING INFLECTION

WHAT CHANGES COMPARED TO LOW-NA

Optics and illumination

- **New 0.55 NA anamorphic optical system:**

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While ASML maintained the EUV wavelength at 13.5 nm, increasing the numerical aperture (NA) was necessary to achieve higher resolution. As a result, NA increased from 0.33 in Low-NA NXE systems to 0.55 in High-NA EXE systems, which required a fundamentally new optical design. Implementing this higher NA meant using larger mirrors, but larger mirrors also increase the angle at which EUV light hits the reticle. At these larger incidence angles, the reticle loses reflectivity, making it harder to transfer the pattern to the wafer. One possible solution would have been to demagnify the mask pattern by 8× instead of the 4× used in NXE systems, but this would have required chipmakers to adopt larger reticles. Instead, **ASML introduced anamorphic projection optics in the EXE platform: the mirrors demagnify the image by 4× in one direction and 8× in the other, rather than shrinking it uniformly.** This reduces the reticle-side incidence angle, avoids the reflectivity issue, and allows High-NA EUV to continue using standard-sized reticles, minimizing disruption to the existing semiconductor ecosystem. However, this design reduces the wafer exposure field to roughly half that of Low-NA EUV (e.g., approximately 26 × 16.5 mm versus 26 × 33 mm). As a result, larger dies may require stitching or additional exposures to be fully patterned. This field-size reduction has a significant impact on throughput, as it increases the number of exposures required per wafer, as discussed later (Exhibit 14, Exhibit 15).

- **Much larger and heavier projection optics / mirror system:**
  Because High-NA collects and projects light over a wider angular range, the optical system becomes much larger than in Low-NA EUV. ZEISS states that the High-NA projection optics contain more than 40,000 parts and weigh around 12 tons, with around 7x the volume and weight of the LNA EUV projection optics. In practical machine terms, this means the EXE platform needs a much larger and more complex optical module than NXE.

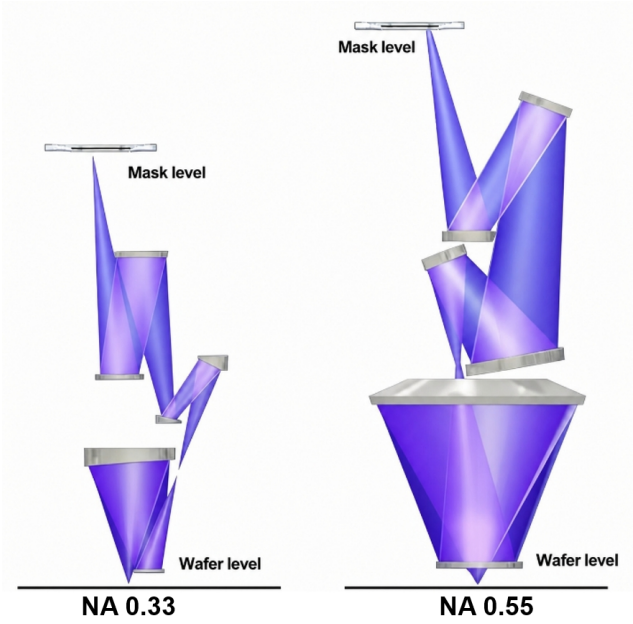
- **Larger illumination system to support the 0.55 NA optical path:**
  High-NA illumination system weighs around six tons, about 4x more than before. This reflects the need to handle the wider angular range associated with 0.55 NA imaging. ASML also highlights a High-NA flexible illuminator roadmap to improve transmission and further support High-NA contrast/resolution scaling.

New EXE platform built around these optics:

- High-NA is implemented on EXE platform, while Low-NA EUV uses the NXE platform. The EXE machine is therefore built around larger HNA optics and adapted illumination enabling 8 nm resolution compared with 13 nm resolution for 0.33 NA EUV. ASML also redesigned the wafer and reticle stages for HNA: the EXE **wafer stage accelerates at 8g, about twice as fast as the NXE wafer stage, while the EXE reticle stage accelerates at 32g, around four times faster than NXE** — equivalent to a race car accelerating from 0 to 100 km/h in 0.09 seconds. Overall, the system is also significantly heavier, increasing to ~300 tons versus roughly 200 tons for Low-NA.

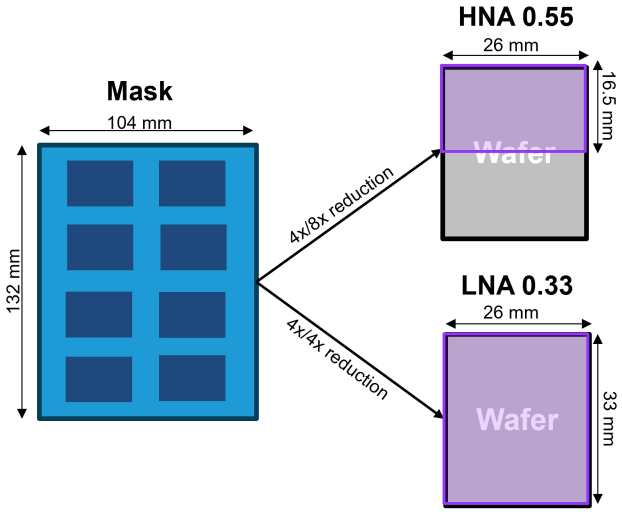
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EXHIBIT 14: **HNA EUV moves to 0.55 NA optics while keeping the same 13.5 nm wavelength, improving demonstrated resolution from ~13 nm to ~8 nm. This higher optical aperture increases image contrast and allows smaller pitches to be printed with fewer patterning steps.**



Source: Company reports, Bernstein analysis

EXHIBIT 15: **In HNA, anamorphic optics use 4× demagnification in one axis and 8× in the other, so the 0.55-NA scanner prints only a half-field on the wafer. Larger logic dies must be split across two mask fields.**



Source: Company reports, Bernstein analysis

HNA ROADMAP

The HNA roadmap started in 2014, when tool design began. The R&D phase then ran for almost a decade, covering design, module manufacturing, integration and qualification. The first EXE:5000 shipment took place in Q4 2023, with Intel as the first customer, marking the transition from R&D into customer testing and learning.

1. **This first phase, called "R&D", focused on imaging capability, process development and performance testing.** The opening of the joint High-NA EUV lab with imec in June 2024 marked a major milestone in High-NA development, enabling broader customer wafer exposure. Customers began using the lab to learn about processes and masks ahead of HVM. By Q3 2024, the first wafer was out in the field, and around 2,000 wafers were exposed by DRAM and foundry customers in the HNA lab by the end of 2024. After Intel, HNA systems were also shipped to Samsung, SK Hynix and TSMC.

2. **From 2025 to 2026, the roadmap entered ASML's second phase, Production Qualification.** This phase focuses on availability, reliability, defectivity, system maturity and cost of technology. In 2025, the key milestone was reaching the 80% availability target. Stitching solutions were also made available to address the HNA half field challenge. In Q1 2026, the first EXE:5200B was qualified. The system achieved 175 WpH, matched machine overlay of ≤0.8 nm, and customer availability above 80%. By early 2026, more than 500k wafers had been exposed on EXE systems. ASML expects multiple EXE:5200B shipments in 2026 and targets 90% availability by Q4 2026.

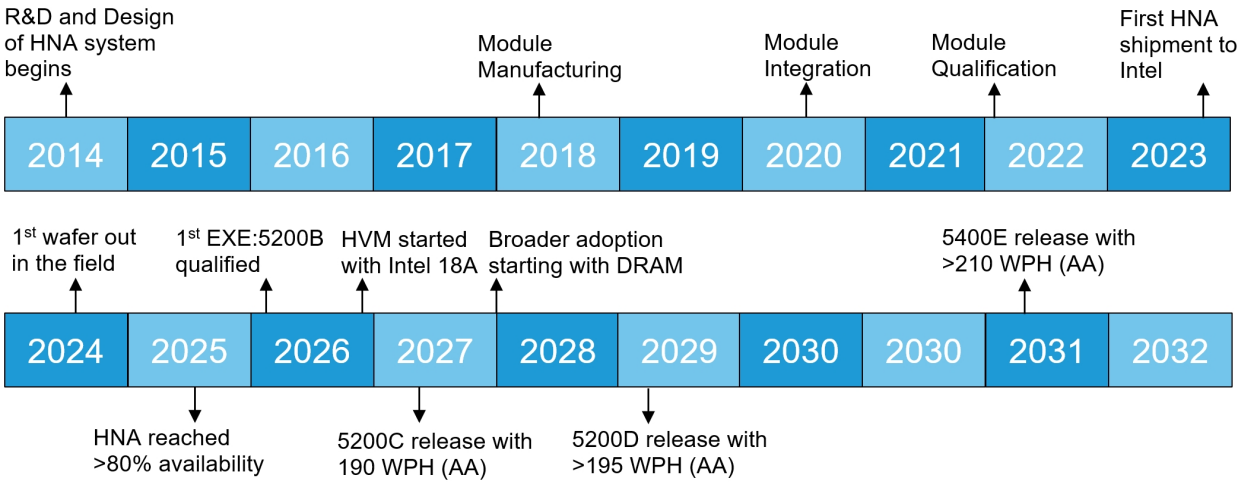
3. The third phase is **High Volume Manufacturing (HVM)**. In this phase, the focus shifts from production qualification to sustained manufacturing performance, including overall equipment efficiency (OEE), cost and operational cost, uptime, stability and manufacturability at scale. While the HVM start had previously been modeled in the 2027 timeframe, Intel and ASML have now disclosed that HNA has entered HVM earlier than expected: Intel Foundry is using HNA on the Intel 18A process node to manufacture a subset of **Intel Core Ultra Series 3 "Panther Lake"** processors, marking the first high-volume logic product using HNA EUV. Specific Intel 18A layers have been dual-qualified on HNA with product shipping to customers at yields matched to the NXE platform. This provides an important readiness milestone for broader adoption,

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while management has also referred to a sizable low double-digit HNA backlog supporting initial insertion, with a larger order wave expected later to support broader HVM adoption across more layers and future nodes.

For HVM, the HNA roadmap moves first to the EXE:5200C in 2027, with MMO <0.8 nm, 190 WpH AA and 160 WpH AB. This improves productivity versus the EXE:5200B, which is listed at 175 WpH AA and 135 WpH AB. The next tool is the EXE:5200D, which keeps MMO <0.8 nm and raises productivity to at least 195 WpH AA and at least 175 WpH AB. The following step is the EXE:5400E, which further improves overlay and productivity, with MMO <0.7 nm, at least 210 WpH AA and at least 180 WpH AB. Later in the roadmap, ASML expects to introduce a high productivity HNA platform around the middle of the next decade, the EXE:5600, with a target of at least 250 WpH (Exhibit 16).

EXHIBIT 16: **HNA development began in 2014 and required nearly a decade to achieve its first shipment in 2023. HVM commenced this year with Intel 18A, and we expect broader adoption in DRAM around 2027. Meanwhile, ASML's long-term roadmap continues to enhance productivity, overlay, and imaging performance through 2032.**



Source: Company reports, Bernstein analysis

HNA BENEFITS

High NA EUV technical values:

- **Higher resolution:** 0.55 NA improves optical resolution versus 0.33 NA, moving from around 13 nm resolution to around 8 nm. **This smaller printable feature size is a core scaling benefit: it enables approximately 1.7x smaller features and up to 2.8x higher pattern density.** In practice, this gives chipmakers more room to shrink critical logic and DRAM patterns without relying on complex multi-patterning. The higher resolution also supports denser cell layouts and more advanced interconnect designs, helping extend EUV scaling for the most critical layers in future technology nodes.

- **Higher imaging contrast:** Higher contrast improves imaging quality, with around 40% improvement in local CDU, 1.4x lower pattern variability and 1.4x lower dose. This directly supports better process control, lower dose requirements and higher effective productivity.

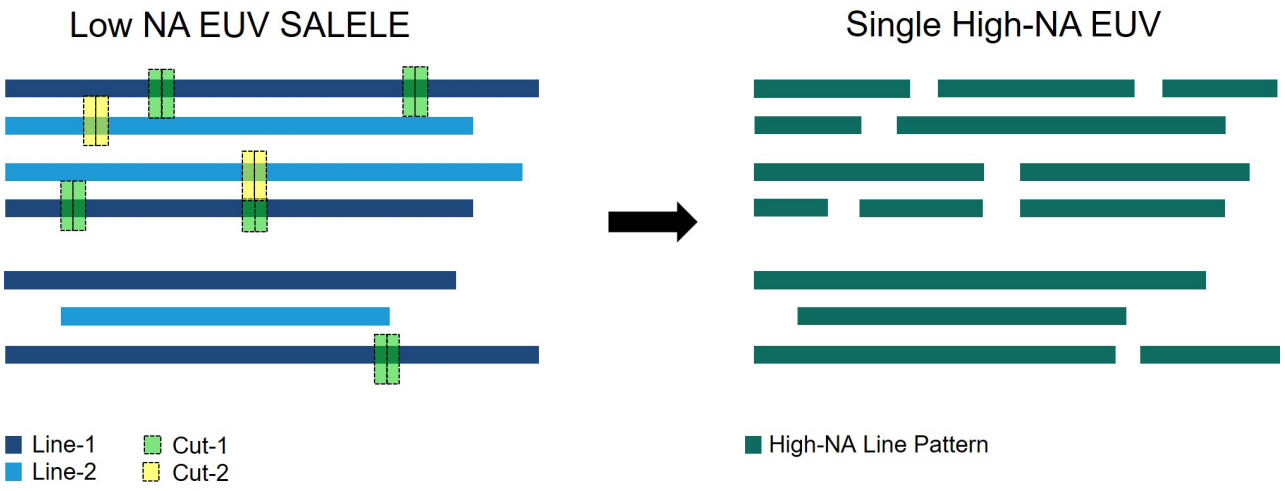
Benefits for customers

- **Patterning cost reduction:** The main customer benefit is lower total patterning cost on critical layers. At very tight pitches, LNA increasingly needs double or triple patterning. HNA can replace LNA multi patterning with single exposure, reducing masks, litho etch loops, non lithography process steps and dose. Demonstrated use cases show around 20% to 35% cost benefit for critical layers, with a roadmap toward more than 20% to 40% patterning cost improvement versus LNA for logic and DRAM applications (Exhibit 17).

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- **Improved yield and lower defect density:** Process simplification reduces defect opportunities. Fewer masks and fewer patterning steps mean fewer chances for overlay errors, etch defects and process induced variability. Higher contrast and improved edge placement error also support better patterning yield.
- **Shorter cycle time:** Reducing masks and process loops shortens manufacturing cycle time. Each mask reduction can save around 1 to 2 days, and Intel demonstrated that a move from three 0.33 NA exposures to one 0.55 NA exposure reduces the steps from around 40 to fewer than 10 steps.
- **2D design flexibility and scaling:** High NA enables more flexible 2D layouts, rather than forcing designers into more restrictive one dimensional multi-layer routing schemes. This can increase logic cell density, improve routing efficiency and potentially reduce the total number of metal layers.
- **Less patterning fab space:** Because High NA reduces masks, exposures and process steps, fewer patterning modules are required for the same critical layer output. This improves fab space efficiency, especially where High NA single exposure replaces Low NA double or triple patterning.

EXHIBIT 17: **HNA simplifies critical layer patterning by replacing low-NA SALELE line/cut multi-patterning with single exposure, reducing masks, litho-etch loops, process steps and non-litho cost, while materially increasing litho intensity.**



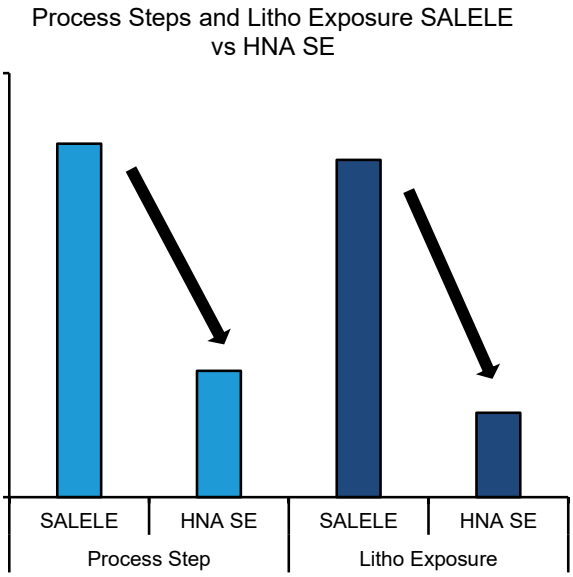
Source: IEEE VLSI Symposium 2026, Bernstein Analysis

Impact for ASML: higher lithography intensity

- **Higher lithography intensity:** High NA shifts value from non lithography process steps into lithography. Even though the customer benefit is lower total patterning cost, a larger share of that cost becomes lithography capex and opex because HNA single exposure replaces multiple LNA litho etch loops and related non lithography steps. ASML estimates around 1.2x higher lithography intensity for single exposure HNA versus LNA multi patterning, while non lithography cost declines. This is strategically important for ASML because HNA does not only enable scaling, but it also increases the lithography share of wafer patterning spend on the most critical layers (Exhibit 18, Exhibit 19).

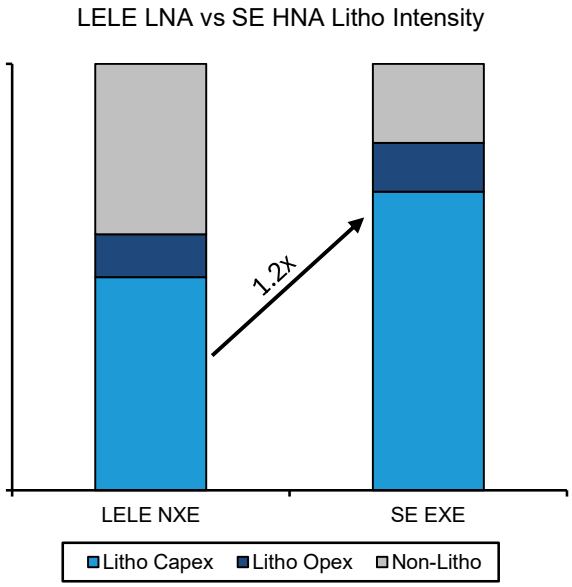
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EXHIBIT 18: **HNA EUV reduces process complexity and lithography exposures compared to SALELE, enabling more efficient patterning, lower cost and improved throughput.**



Source: IEEE VLSI Symposium 2026, Bernstein Analysis

EXHIBIT 19: **ASML estimates a significant increase in litho intensity when transitioning from LELE LNA to single-exposure HNA. Litho CapEx and OpEx are expected to rise by approximately 1.2×, while non-litho costs are projected to decline.**



Source: ASML, Bernstein analysis

HNA CHALLENGES

- **Half field:** As we mentioned, HNA can expose only half the field of LNA. This is a direct consequence of the anamorphic optical design used in EXE systems: HNA keeps the standard mask format but uses different demagnification in x and y, which results in a half-field exposure on wafer versus the full-field exposure of LNA NXE. This creates two direct issues compared with LNA:

    1. **Throughput pressure from half-field exposure:** Even when the die layout fits within a half-field (16.5x26mm), the same mask may need to be exposed across roughly twice as many fields to cover the entire wafer, creating a throughput penalty. Consequently, EXE productivity is significantly lower than NXE because each exposure covers a smaller wafer area (Exhibit 20).

    2. **Stitching for large die:** The half-field limitation is particularly significant for large logic dies, where the die may not fit within a single EXE half-field. In such cases, the layout may require an AB split, with part of the pattern assigned to one mask field (A) and the remainder to another (B), followed by on-wafer stitching. This is more than a layout inconvenience: the stitch boundary must maintain overlay accuracy, CD continuity, and image integrity at device-relevant dimensions. Consequently, this approach introduces additional complexity and further impacts productivity.

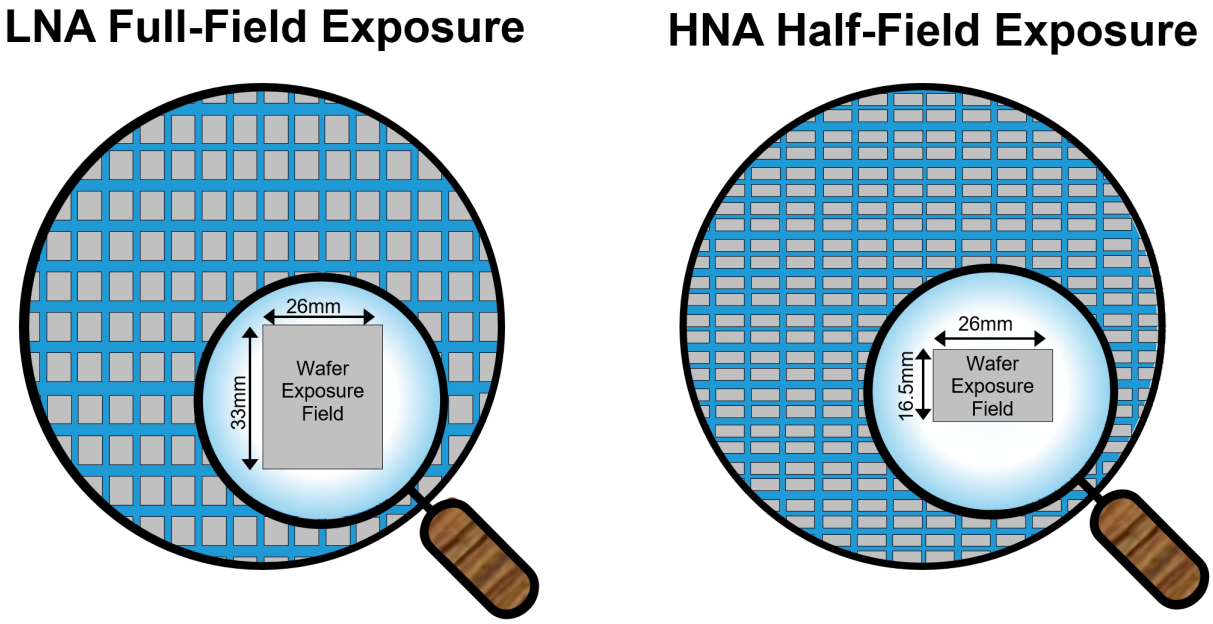
- **Depth of Focus (DoF):** HNA has a smaller effective depth of focus than LNA because DoF scales approximately with wavelength divided by NA squared. Moving from 0.33 NA to 0.55 NA therefore reduces the focus margin by roughly a factor of 2.5 to 3. This means HNA is more sensitive to wafer topography, focus errors, film-stack variation, resist thickness and leveling accuracy. In practical terms, the process has less vertical margin: a wafer area that would still print acceptably on Low-NA may move outside the usable focus window on HNA. This is one reason thinner resist films, optimized underlayers, optimized pupils and 3D resist/process optimization become more important.

- **Faster wafer and reticle stage dynamics:** High-NA's half-field architecture requires faster wafer and reticle stages to recover productivity. The stages must move faster while still preserving overlay and imaging stability. That implies tighter wafer-reticle synchronization, stronger control of vibration during scanning, and careful management of heat and mechanical

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stability in high-dynamic moving modules.

EXHIBIT 20: **The HNA throughput penalty: full-wafer coverage requires ~2× more field exposures than NXE, significantly reducing productivity because each exposure covers a smaller wafer area.**



Source: Company reports, Bernstein analysis

PRODUCTIVITY

Half Field Exposure: The Structural Drag

As we explained, HNA throughput is structurally lower than LNA throughput because the EXE optical architecture uses half-field exposure. The anamorphic optics limit the printable exposure field to half the field used in NXE systems, so the scanner must expose more fields to cover the same wafer area. For logic, throughput can be even lower because large dies may require the pattern to be split across two masks (AB) and stitched together, which further reduces throughput.

ASML partially offset the Penalty

- The EXE platform was designed to compensate for the half field penalty with faster motion. **The key response was to increase wafer and reticle stage acceleration so the tool can move faster from field to field**. ASML explains that, because HNA must expose more fields, the system was designed with faster stages to offset the extra field count. The wafer stage accelerates at 8g, around twice the NXE wafer stage, while the reticle stage reaches 32g, around 4x the NXE reticle stage. This does not remove the half field penalty, but it materially reduces the throughput loss that would otherwise come from exposing more fields per wafer (Exhibit 21).

- **The second offset is lower dose from better image contrast.** HNA delivers higher contrast, which can reduce dose requirements and therefore raise productivity. ASML demonstrated that HNA produces better local CDU and pattern integrity at lower dose than LNA in comparable critical layer use cases. This is important because throughput scales with how much dose is required per exposure. Better contrast therefore partly offsets the higher field count by reducing the photon budget needed per field.

- Specifically for AB exposures, **the wafer handler stocker further improves throughput** by reducing reticle exchange overhead. On EXE:5200B, AB throughput improves to 135 WpH at 50 mJ/cm² by enabling up to 25 wafers to be exposed in an AABB sequence, rather than exchanging reticles every wafer in an ABBA sequence.

Future improvements, but HNA remains below LNA

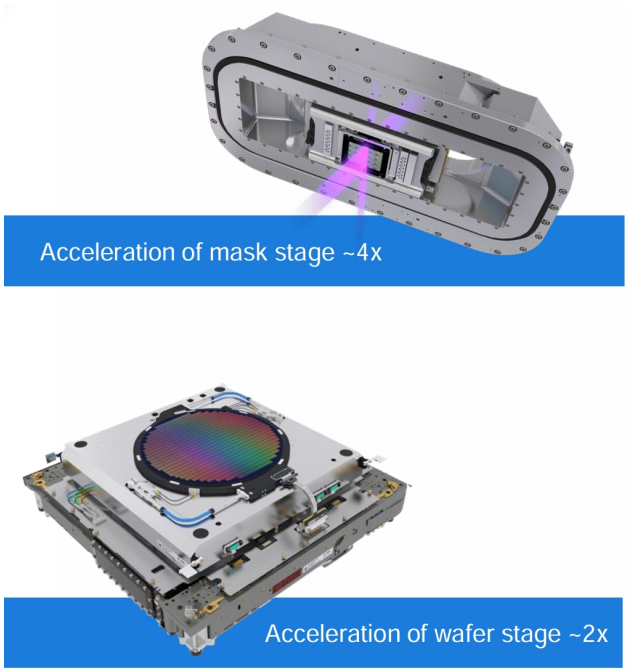
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- **Source power has always been the most important lever for EUV productivity improvement**, across both LNA and HNA, and it will continue to be the main driver of throughput gains. This was already visible with EXE:5200B where throughput increased to 175 WpH on EXE:5200B from 110 WpH on EXE:5000, supported by a 102% increase in source power. The roadmap then targets around 190 WpH on EXE:5200C, at least 195 WpH on EXE:5200D and at least 210 WpH on EXE:5400E for AA, while AB remains lower at around 160 WpH, at least 175 WpH and at least 180 WpH respectively. This impressive throughput gain will be mainly driven by source power. EUV source power is moving from today's 500 to 600 watt range to 740 watts already demonstrated, and now to a disclosed 1,000 watt capability (more details in this report: ASML: LNA EUV ASP seeing 60% upside? Outperform). More source power means more photons, shorter exposure times and higher WpH (Exhibit 22).

- **The second lever is optical transmission.** A future HNA flexible illuminator is expected to increase total system transmission by around 1.4x, allowing more useful photons to reach the wafer for the same source power. This should further improve HNA productivity and help drive cost per exposure lower.

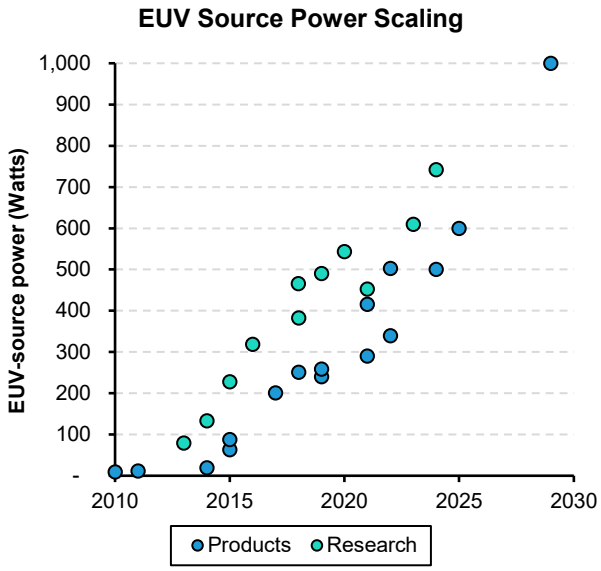
However, these improvements narrow the gap rather than eliminate it. HNA remains structurally below LNA on scanner throughput because the half field architecture remains. The roadmap shows LNA moving toward 300 WpH and 330 WpH on later NXE systems, while HNA reaches just over 210 WpH on the current EXE roadmap (Exhibit 23).

EXHIBIT 21: **ASML designed HNA with significantly faster stages to compensate for the increased number of exposure fields, doubling wafer-stage acceleration to 8g and quadrupling reticle-stage acceleration to 32g versus LNA.**



Source: ASML

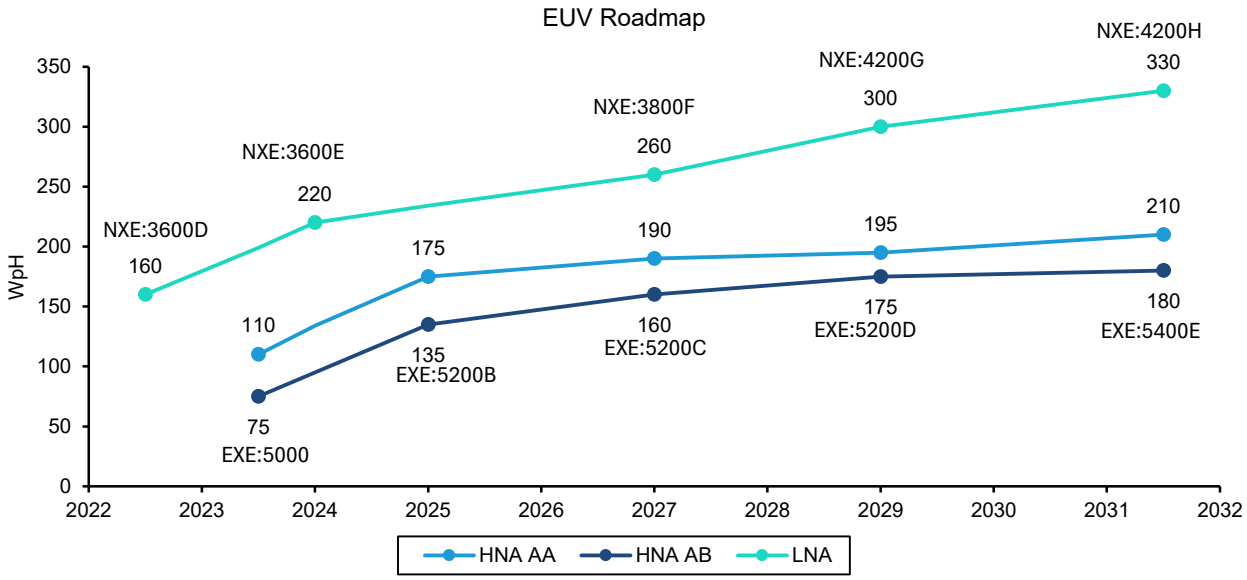
EXHIBIT 22: **ASML had already presented a roadmap at its 2024 Investor Day indicating that EUV source power is expected to reach 1,000 W around 2030. In February 2026, the company demonstrated a path to achieving this milestone by the end of the decade.**



Source: Company reports, Bernstein analysis and estimates

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EXHIBIT 23: **HNA EUV throughput improves through faster stages, lower dose requirements and higher source power, but the half-field exposure architecture remains a structural constraint, leaving scanner productivity materially below LNA despite continued roadmap advances.**



Source: Company reports, Bernstein analysis and estimates

PHOTORESIST FOR EUV

Photoresist and underlayer development are central to HNA because the scanner's optical advantage only matters if the resist stack can convert higher resolution and higher contrast into stable wafer patterns. The focus is on screening alternative resist materials with suppliers and benchmarking defectivity, roughness and dose reduction.

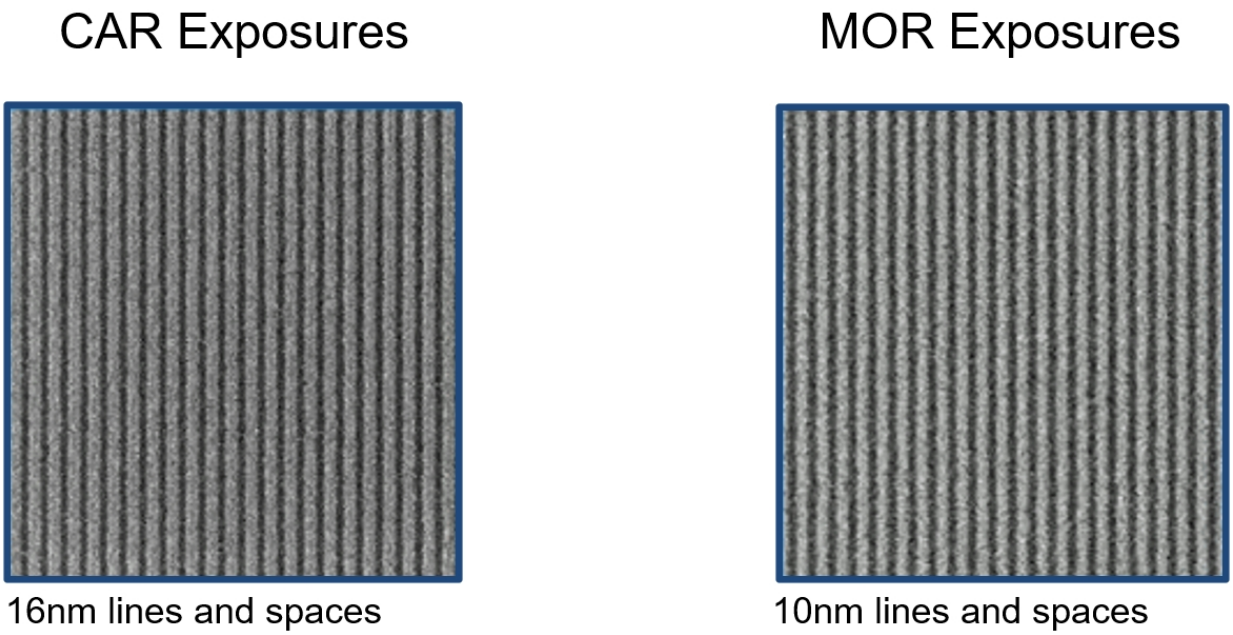
Chemically amplified resist (CAR) has dominated optical lithography for decades and should continue to be used for selected HNA applications. HNA has already shown strong results with CAR, including 16 nm lines and spaces resolved in early HNA patterning work, while optimized CAR resist has also shown improved LCDU performance for 28 nm pitch DRAM contact holes. However, HNA may also create a broader opportunity for metal oxide resist (MOR). **In 2024, IMEC demonstrated that MORs deliver strong performance at smaller feature sizes by successfully printing 10 nm lines and space**. MORs are therefore expected to play an increasingly important role as the industry moves toward tighter pitches and lower stochastic variability (Exhibit 24).

The key challenge is not only resolution. The resist stack must balance resolution, line edge roughness and sensitivity, or speed. Improving only resolution and roughness can slow the scanner, while HNA economics depend on maintaining good pattern quality at acceptable dose and throughput. The latest HNA resist results show why this matters. For 28 nm pitch DRAM contact holes, resist optimization is being used to address the depth of focus challenge, with optimized CAR showing around 40 nm visual DoF and improved LCDU results across different resist options ~1.5nm LCDU. Positive tone MOR with PT dry develop achieved 1.3 nm LCDU at 3σ, enabling further shrink, with 3D resist optimization identified as the next step.

Underlayers are another important knob. Matching the underlayer to the resist can improve adhesion, and the right underlayer and resist combination can help reduce exposure dose. Lower dose matters because it directly supports higher productivity and lower HNA EUV cost.

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EXHIBIT 24: **IMEC demonstrated that an HNA scanner achieved 16 nm feature resolution with a chemically amplified resist (CAR), whereas the use of a metal oxide resist (MOR) enabled the resolution of features as small as 10 nm.**



Source: IMEC, Bernstein analysis

6"×12" MASKS: A PATH BEYOND STITCHING

Larger masks could eventually eliminate one of HNA's biggest drawbacks: stitching. Today, both LNA and HNA EUV use the industry's standard **6" × 6" reticle format**, which has remained largely unchanged for decades and underpins the entire mask ecosystem, including mask blanks, writers, inspection tools, pellicles, reticle pods, stockers and scanner handling systems. Maintaining this standard was one of the key reasons ASML adopted anamorphic optics for HNA, avoiding a disruptive change to the existing infrastructure.

The most frequently discussed long-term solution is a transition to a 6" × 12" mask format. Intel has been the strongest advocate of this approach, and industry groups have already begun evaluating the required infrastructure, including larger mask blanks, carriers and handling systems. A 6" × 12" reticle would effectively restore the lost field dimension created by HNA's anamorphic optics, allowing many large logic dies to be printed within a single exposure field without stitching. While even larger formats such as 12" × 12" are occasionally discussed, industry activity today remains overwhelmingly focused on 6" × 12", making it the most realistic path should the ecosystem decide to move beyond the current 6" × 6" standard.

The challenge is that changing mask size would require a coordinated upgrade across the entire semiconductor ecosystem. Larger defect-free EUV mask blanks would need to be manufactured, pellicles redesigned, mask writers and inspection tools upgraded, and fabs would require new reticle transport, storage and handling infrastructure. This ecosystem-wide cost and complexity is the main reason the industry initially chose to retain the 6" × 6" mask standard and accept the half-field limitation of HNA.

If adopted, larger masks would improve throughput even beyond eliminating stitching. Removing AB stitching would avoid dual-mask exposures, reticle exchanges and stitch-overlay control, while simultaneously increasing the exposed wafer area per scan. **As a result, more die could be printed per exposure, improving scanner productivity and reducing cost per layer.** In effect, a larger mask could address both major consequences of HNA's half-field architecture: stitching complexity and the associated throughput penalty.

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HNA COST ANALYSIS AND ADOPTION

HNA delay has been one of the concerns from investors, notably by TSMC (ASML - High-NA EUV adoption postponed?). Investors often ask why HNA has not been more widely adopted and whether this reflects a slowdown in lithography relative to other process steps such as etch and deposition. However, the recent news that Intel has adopted High-NA EUV for its 18A process demonstrates that the technology is ready for high-volume manufacturing and that adoption is now underway. We believe Intel's deployment should pave the way for broader industry adoption over time. **We've analysed the HNA cost vs. LNA EUV, and conclude that while Intel has taken an early lead in adopting HNA, broader adoption is likely to occur first in DRAM, followed by logic, which drives an increase in litho intensity.**

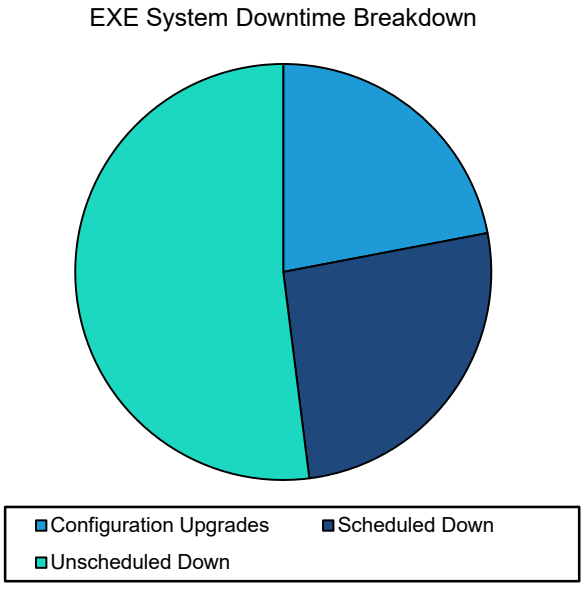
Cost of HNA exposure is high now but is expected to come down significantly as availability improves. We estimate with 95% availability cost for HNA exposure can drop by 23%.

- **Current low tool availability:** At the current stage, HNA tools suffer from lower availability, which is a common issue for a new litho tool. While HNA is already progressing through the expected maturity curve, running at ~80% availability in 2025, this is still meaningfully below LNA which reached close to 95% availability. By Sep-2025, EXE systems had exposed more than 500k wafers, providing a much larger data set to drive reliability learning and HVM readiness.

- **Improving availability in sight:** ASML disclosed that HNA availability reached above 80% for the first time in 2025, with fleet availability maturing toward a 90% target in 2026. The main source of lower availability remains long unscheduled downs, especially >12-hour events, while scheduled downtime is also partly driven by monitoring, configuration updates and platform learning. ASML's maturity curve shows EXE availability tracking favorably versus LNA/NXE at a comparable stage, targeting ~95% over the next 3-4 years (Exhibit 25), (Exhibit 26).

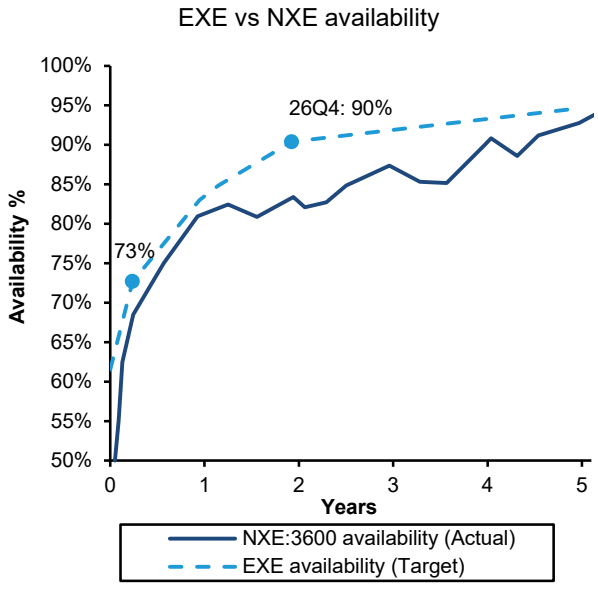
- **Cost-per-exposure drops:** With higher availability, we estimate the litho equipment cost for HNA exposure can drop by 23% from 2025-2030. Higher availability is an important lever, but not the only driver of HNA cost reduction. Cost per exposure also improves with throughput: EXE:5200B has achieved 175 WpH in AA, up from 110 WpH on EXE:5000, with ASML's roadmap moving toward 190+ WpH (Exhibit 27).

EXHIBIT 25: **Unscheduled downtime is the primary driver of EXE unavailability and reducing it is the critical path to achieving the 90% availability target.**



Source: Company reports, Bernstein analysis

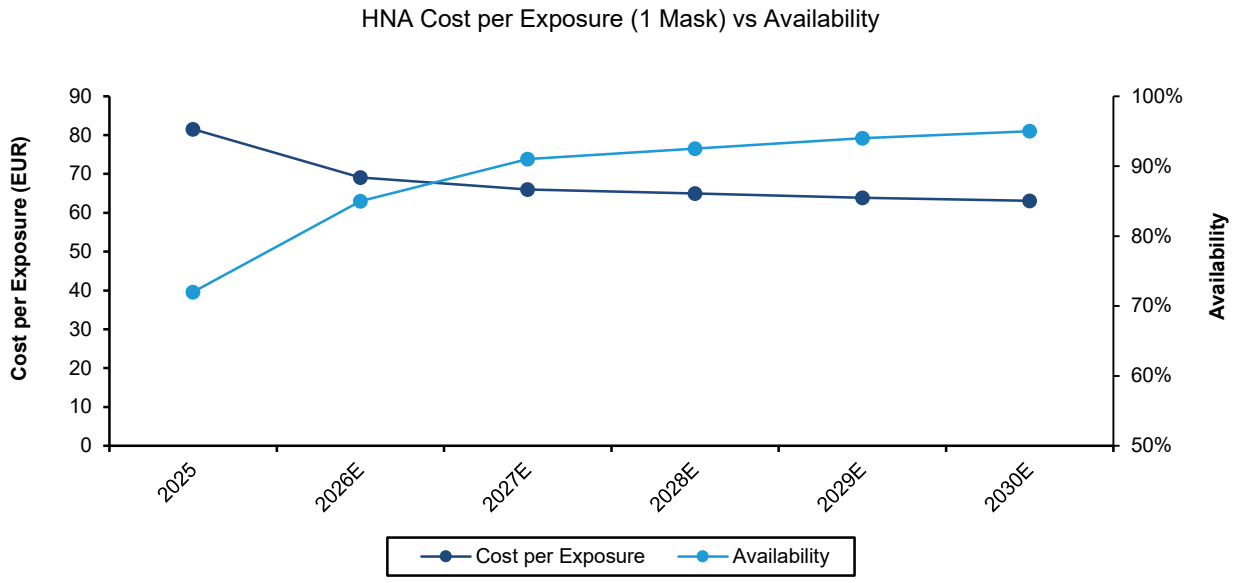
EXHIBIT 26: **EXE availability is targeted to reach 90% by 26Q4 and converge with the NXE:3600 mature fleet performance of 95% over five years**



Source: Company reports, Bernstein analysis.

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EXHIBIT 27: **With HNA availability reaching 95% the cost of a HNA exposure drops by 23%, from ~82€ to ~63€.**



Source: Company reports, Bernstein analysis and estimates.

However, HNA exposure cost is not the same for all. As we mentioned in the sections above, HNA throughput (and hence cost) gets impacted from half field stitching, which results in slower throughput & higher cost for larger dies.

- **For products with many small die, such as some DRAM or smaller logic die, this is manageable:** the scanner can expose twice as many half-fields using the same mask, with no need to stitch a single large die. For a single large logic die such as GPU dies, however, the chip can exceed one EXE half-field. In that case, stitching will be required. In simple words, stitching means splitting a large die across two EXE half-field exposures (Mask A and Mask B), and designing an overlap/ stitch zone where the two exposures connect. The chip floorplan and routing are then made stitch-aware, so layout features crossing the boundary can be connected while controlling overlay and placement errors (Exhibit 28, Exhibit 29).

Our simulation shows that the cost for HNA is significantly lower for smaller dies than larger dies due to stitching, especially in the first few years.

- For larger dies, HNA's half-field exposure requires two reticles (AB) and die stitching, which lowers effective throughput versus AA exposures where the same reticle can be reused. ASML's roadmap shows this clearly: The current EXE:5200B runs at **175 WpH in AA** but **135 WpH in AB**, a ~23% reduction.

- This results in a big difference in HNA exposure cost; based on our calculation, the litho equipment cost for each HNA exposure is 2.4x of LNA with 1 mask (AA) and 3.1x of LNA with 2 masks (AB) in 2025.

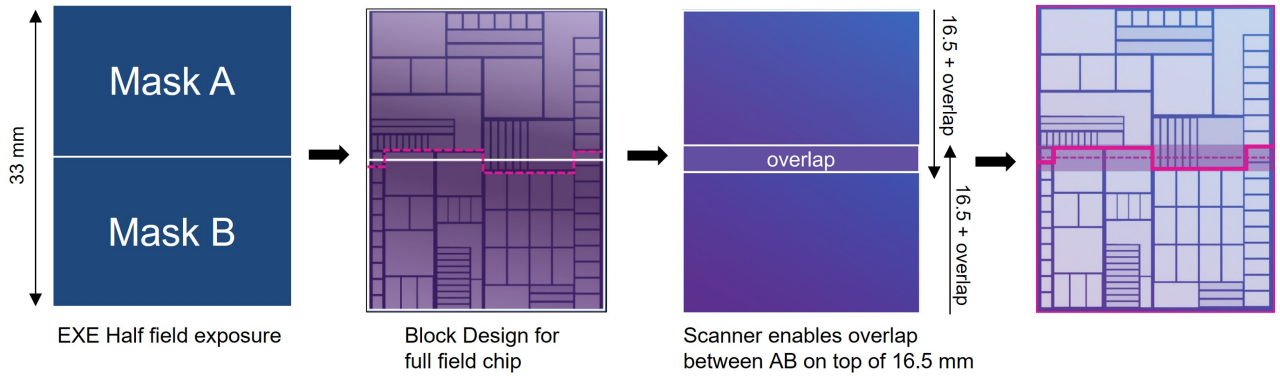
- The gap between AA and AB is narrowing. Next gen EXE:5200C improves to **190 WpH AA** and **160 WpH AB**, narrowing the gap to ~16%. The roadmap then points to further productivity gains, with EXE:5200D at ≥195 WpH AA / ≥175 WpH AB and EXE:5400E at ≥210 WpH AA / ≥180 WpH AB (Exhibit 30).

- This means the litho equipment cost for HNA reduces overall, and the cost gap between larger dies and smaller dies narrows. By 2030, with the expected availability improvement, we expect the difference narrows to 1.9x for HNA AA and 2.1x for HNA AB, with still a significant gap between HNA AA and AB. (Exhibit 31)

- This means that for smaller dies (most typical example would be DRAM), HNA litho equipment cost of exposure is lower and is easier to justify, compared to larger dies. For larger dies, HNA litho equipment is only lower than complex EUV double patterning or 3x patterning, or over time when HNA cost comes down further. However, the trend of migration to HNA doesn't change.

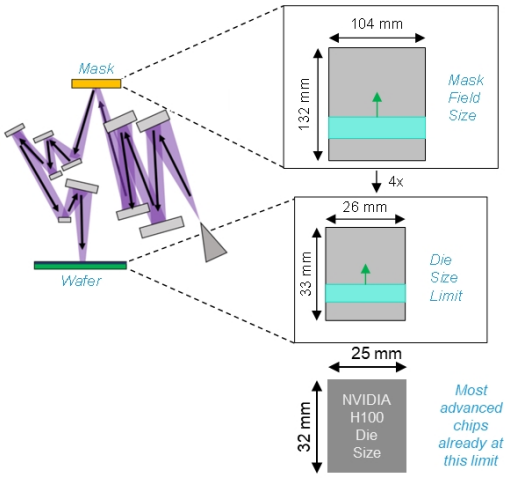
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EXHIBIT 28: **In the die-stitching process, a large die is divided into two half-field exposures that are subsequently joined through a carefully designed overlap region. This approach enables seamless integration of blocks, continuous routing across the boundary, and accurate alignment between the two exposures, allowing them to function as a single chip.**



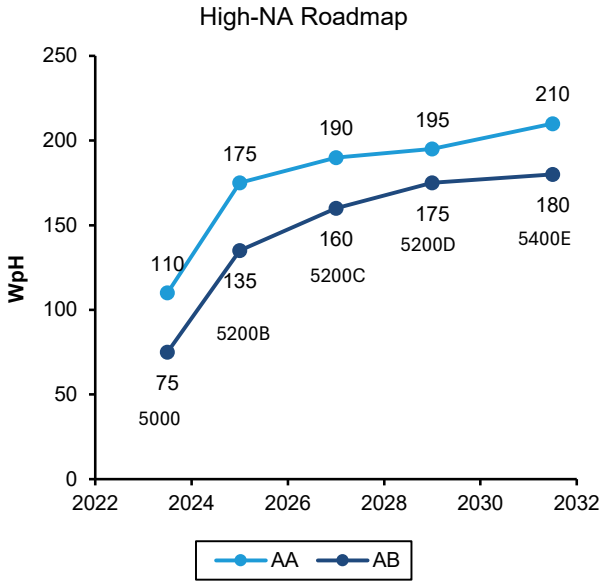
Source: ASML, IMEC, Intel, Bernstein analysis

EXHIBIT 29: **The H100/B100 GPU die size is already approaching the physical reticle limit of 33 × 26 mm². With HNA, this limit is reduced to 16.5 × 26 mm². Consequently, large logic dies require stitching.**



Source: ASML, Nvidia, Bernstein analysis.

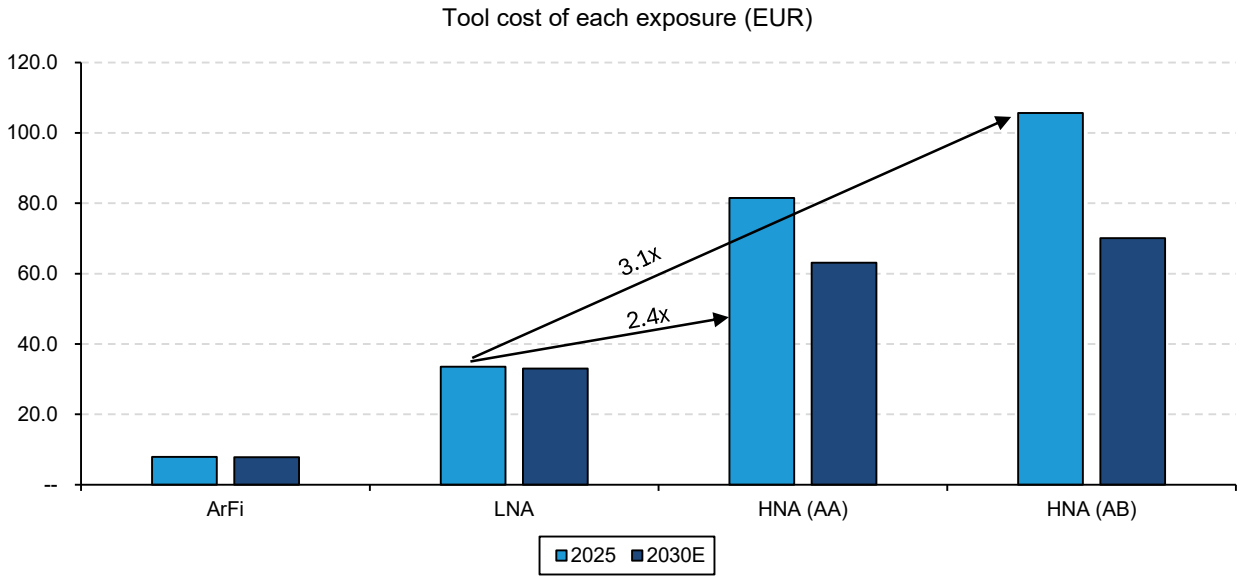
EXHIBIT 30: **AB HNA throughput is expected to remain materially lower than AA over the next decade, driven by the requirement for dual masks and stitching.**



Source: Company reports, Bernstein analysis

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EXHIBIT 31: **Due to the lower throughput of AB HNA, the litho equipment cost per exposure is approximately 3× that of a LNA exposure, while for AA HNA the cost is only about 2.4× that of LNA. We expect these costs to decline by 2030 to around 2.1× and 1.9×, respectively.**



Source: Company reports, Bernstein analysis and estimates.

We conclude that it's likely for DRAM to adopt HNA earlier than logic, due to the absence of mask changing.

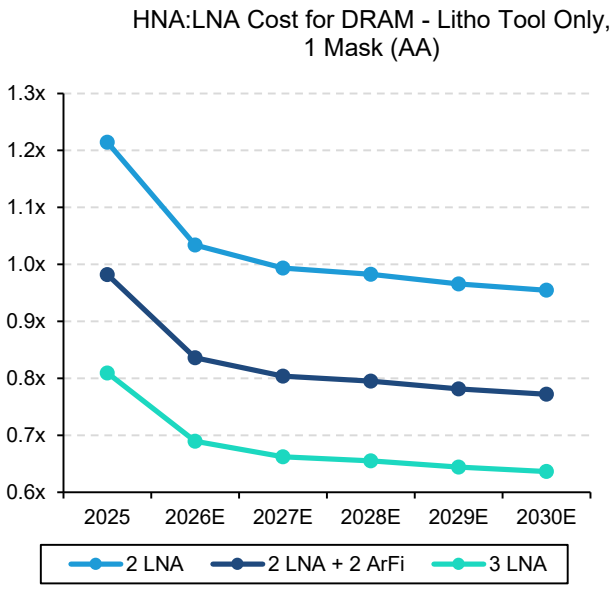
- Based on the logic and DRAM roadmaps, HNA adoption becomes viable for logic at A14 (2027/28) and DRAM D1d (2027).
- Our simulation shows that for DRAM, HNA is almost certainly cheaper than LNA LELE double patterning. The gap widens when considering more complex SALELE with 4 exposures (2x LNA EUV and 2x ArFi), or LNA EUV LELELE (3x LNA EUV). (Exhibit 32)
- However, for large logic die requiring stitching (AB), it is only justifiable over time to replace SALELE with either 2x EUV + 2x ArFi or 3x EUV. In fact, although the litho equipment cost ratio between HNA SE and 2 LNA decreases significantly, by around 50% from 1.6x in 2025 to 1.1x, it will still remain cheaper to use double exposure LNA rather than single exposure HNA over the next five years (Exhibit 33)

The above analysis only considered the cost of litho tool itself. There are other factors to consider. Considering the total cost, we believe HNA will be more cost competitive as availability increases, even for larger logic dies.

- **HNA also drives overall process simplification, non-litho cost cuts, yield improvements, hence should drive higher Litho Intensity.** HNA enables process simplification because its higher resolution and contrast allow critical layers that would otherwise require LNA EUV multi-patterning — e.g., line/cut split flows such as SALELE — to be printed with a single HNA exposure. This reduces the number of masks, litho-etch loops, cut steps and related non-litho processing, while also improving pattern fidelity, local CDU and defectivity.
- **This simplification shifts value from non-litho processing into lithography:** even if the HNA exposure itself is more expensive, the total process flow can become cheaper and more productive. As availability, throughput and ecosystem cost roadmaps improve, HNA should therefore support higher litho intensity, because customers replace complex non-litho-heavy patterning schemes with more lithography-enabled single-expose solutions, including for larger logic dies where stitching solutions are available.
- Considering the total cost, we believe HNA will be more cost competitive as availability increases, even for larger logic dies.

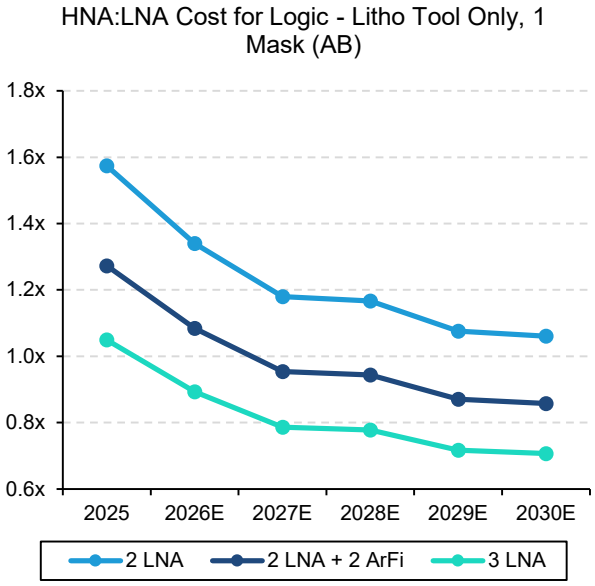
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EXHIBIT 32: **We estimate that, for DRAM, HNA is more cost-effective than LNA LELE double patterning. The advantage becomes more pronounced when considering more complex schemes, such as SALELE with 4 exposures (2× LNA and 2× ArFi), or LNA LELELE (3× LNA).**



Source: Company reports, Bernstein analysis and estimates

EXHIBIT 33: **However, for logic, we estimate that HNA is economically justified only for replacing SALELE with 2× EUV + 2× ArFi or 3× EUV over time.**



Source: Company reports, Bernstein analysis and estimates

As a result, DRAM is likely to see earlier adoption of HNA, with broad deployment beginning at the 1d node in 2027, slightly ahead of logic, which is expected to adopt the technology between 2028 and 2030.

- **Our best guess of HNA adoption is: Intel in 2026 (18A), Samsung / Hynix DRAM in 2027 (D1d), Samsung logic and TSMC in 2030 (A10).** The recent confirmation that Intel is using High-NA EUV for its 18A process demonstrates that the technology is ready for high-volume manufacturing and removes a key uncertainty around adoption timing. That said, we continue to believe the broadest and most compelling economic case for HNA is in DRAM, where patterning complexity and lithography intensity are increasing rapidly. SK hynix has the clearest early signal: the company announced in September 2025 that it had assembled ASML's TWINSCAN EXE:5200B, the first production-oriented HNA system, at its M16 fab for next-generation DRAM development. Samsung is also moving quickly, with industry reports indicating that it ordered two ASML EXE:5200B tools, with the first expected by late 2025 and the second in H1 2026. There is no official HNA disclosure from Micron yet, but they could adopt HNA slightly later, consistent with its more conservative EUV LNA strategy in DRAM. In logic, Intel remains the frontrunner in HNA adoption. The company received the industry's first commercial HNA EUV system from ASML in 4Q23 and, as we mentioned, is already using it in HVM on its 18A process. We expect HNA usage to expand further with the A14 node as Intel moves toward broader production deployment. In contrast, Samsung and TSMC appear to be taking a more cautious approach, with recent reports indicating that meaningful HNA adoption is unlikely before their A10-class nodes around 2030 (Exhibit 1, Exhibit 2, Exhibit 34).

- TSMC and Samsung announcements to adopt HNA slower than Intel doesn't change the view that HNA is better. It probably reflects 1. TSMC's prudence and conservativeness to adopt new technologies vs. optimizing existing technologies, and 2. Economically it's better to wait for HNA to further improve in availability and throughput, which results in lower cost per exposure (but at the risk of not benefiting from HNA immediately).

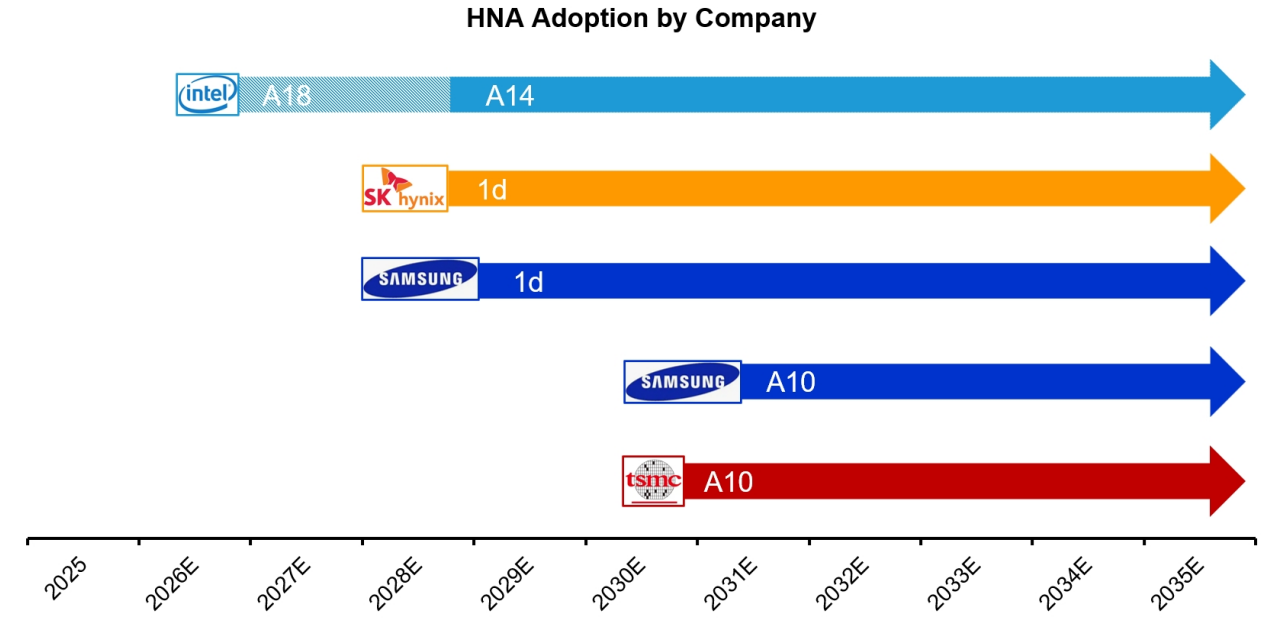
Financially, slower HNA adoption is probably even better for ASML… at least in the near term.

- As shown above, from litho tool perspective, it's economically better to sell more LNA EUV machines than fewer HNA machines. This is especially the case when considering the much higher margin for LNA over HNA EUV.

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- On the other hand, HNA adoption will further increase litho intensity and hence ASML's market share in WFE, as more value goes from non-litho steps (etch, depo, cleaning, etc) to litho when 1 HNA replaces multiple LNA-ArFi steps.

EXHIBIT 34: **Logic HNA adoption has already been validated by Intel at 18A. We expect DRAM adoption to begin with SK hynix and Samsung at 1d, while broader logic adoption is likely at Intel A14. Samsung and TSMC are both expected to introduce HNA around their A10-class nodes near 2030.**



Source: Company reports, Bernstein analysis and estimates

LITHO INTENSITY IMPROVEMENT DRIVEN BY HNA

We expect litho intensity to increase in DRAM, and remains elevated in logic. Overall litho intensity is going up from 24% to 26%.

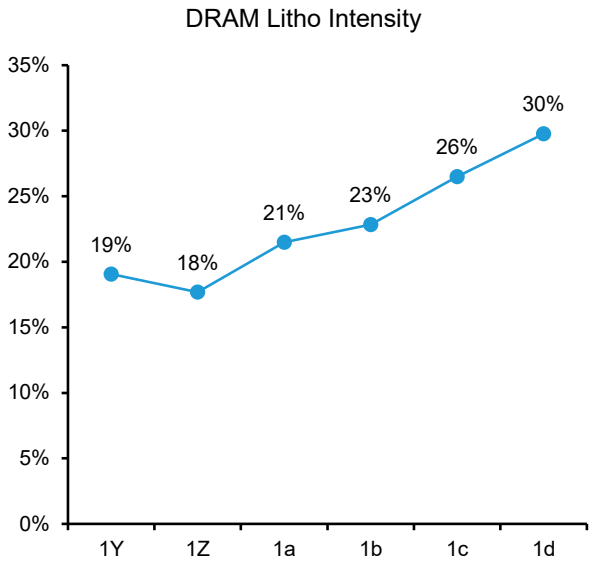
- We estimate litho intensity in DRAM increased from around 20% in 1Y and 1Z to 26% in 1c. This significant growth was driven by the rising number of EUV exposures, starting with 3 to 4 exposures in 1a, increasing to 4 to 6 in 1b, and then to 6 to 7 in 1c. With 1c penetration expected to increase substantially over the next few years, we expect total DRAM litho intensity to grow considerably. Additionally, with the introduction of double patterning EUV or HNA at the 1d node, we expect litho intensity to rise further to around 30% (Exhibit 35).

- Similarly, logic litho intensity increased significantly from around 20% at 10nm, driven by a sharp rise in EUV exposures, peaking at 5nm and 3nm at above 35% intensity. While logic litho intensity declined from 3nm to 2nm due to the adoption of GAA, which requires more non litho steps, it remains elevated at around 32%. We expect it to stay at similar levels or higher with HNA at 1.4nm, and to increase further at the 1nm node (Exhibit 36).

- Blended litho intensity for ASML is increasing and is expected to continue its upward trend, driven by the faster growth of DRAM and advanced logic relative to the overall semiconductor market. Both segments carry considerably higher litho intensity compared to mature logic and NAND, supporting a structurally higher blended litho intensity over time (Exhibit 37).

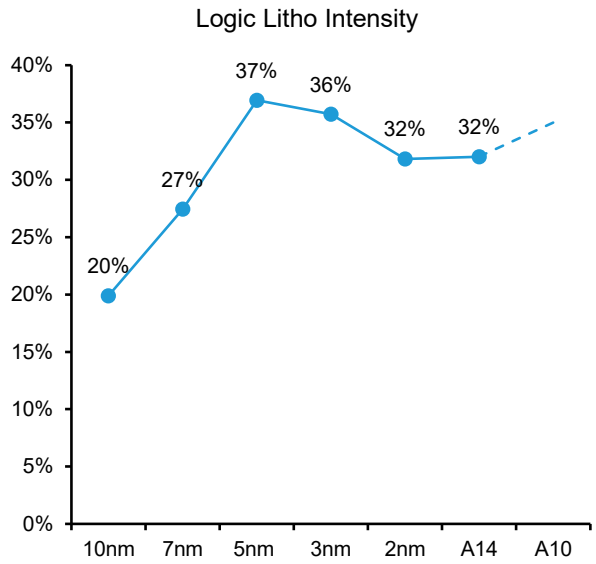
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EXHIBIT 35: **We anticipate an increase in lithography intensity in DRAM. The introduction of double-patterning EUV (or HNA) at the 1d node is expected to drive lithography intensity up to ~30%**



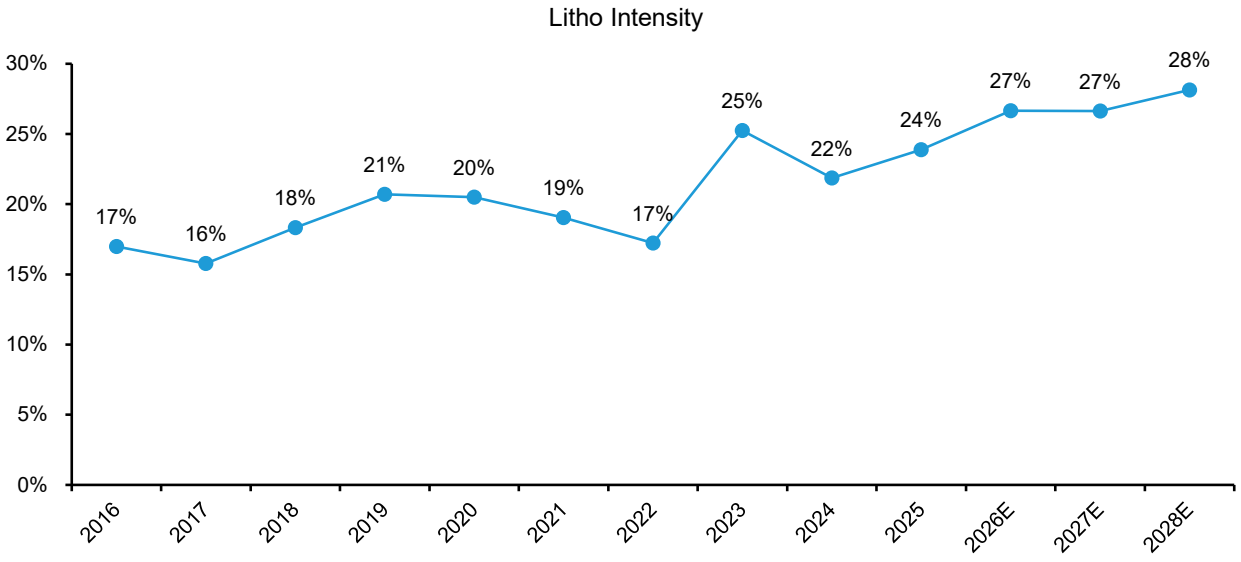
Source: Company reports, Bernstein analysis and estimates

EXHIBIT 36: **Logic litho intensity declined from 3nm to 2nm but remains elevated at ~32%. We expect it to stay at similar levels or increase further with HNA at 1.4nm, and likely rise again at the 1nm node.**



Source: Company reports, Bernstein analysis and estimates

EXHIBIT 37: **We expect litho intensity to continue its upward trend, driven by the increasing penetration of 1c and 1d nodes in DRAM, which command higher litho intensity, as well as advanced logic, which has considerably higher litho intensity compared to mature logic**



Source: Company reports, Bernstein analysis and estimates

LOGIC SCALING SHIFTS FROM LNA MULTI PATTERNING TO HNA

As logic scales beyond the 2nm node, the bottleneck increasingly shifts from transistor architecture to the ability to pattern dense interconnect layers. Metal lines, vias and local interconnects continue to shrink, while edge placement error does not improve at the same pace. Once logic metal pitch moves below roughly 26nm, 0.33 NA EUV increasingly needs multi patterning

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to print the most critical layers. This adds masks, litho etch loops, overlay requirements, defect opportunities and cycle time. HNA addresses this by extending single exposure EUV into pitches where 0.33 NA would otherwise require double or triple patterning.

Why HNA Matters for Logic

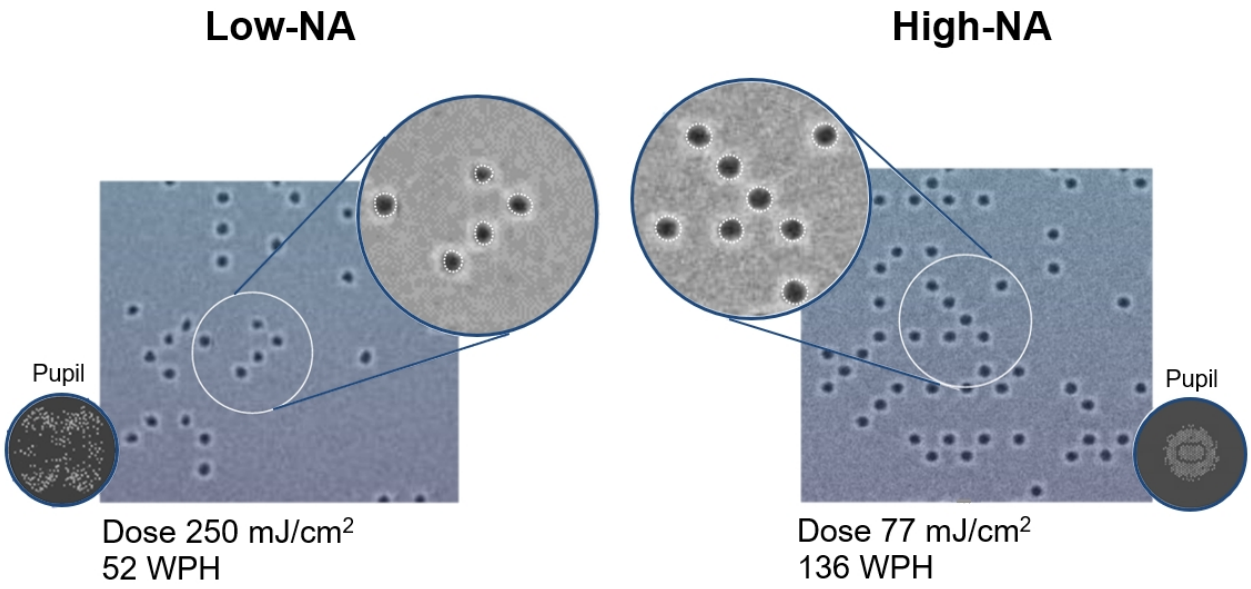
The main benefit of HNA in logic is not only the move from around 13nm resolution to 8nm resolution. The more important advantage is higher contrast. Better contrast produces sharper aerial images, tighter local CD uniformity and lower pattern variability, which are critical for metal and via layers where small placement or dimension errors can create yield loss.

- **P36 Logic Via: Better Imaging at Much Lower Dose.** For a logic via layer with 18nm holes at 36nm pitch, LNA required a 250 mJ/cm² dose and delivered only 52 WPH, while still showing deformed contact holes. ASML demonstrated that HNA can print defect free contact holes at 77 mJ/cm² and deliver 136 WPH. This matters because logic vias are highly sensitive to stochastic defects and local CDU. HNA therefore improves both imaging quality and productivity, rather than forcing a trade-off between the two (Exhibit 38).

- **P30 Random Via: From Double Exposure to Single Exposure**. At P30, HNA can replace a double exposure LNA EUV process with a single exposure HNA flow. This delivers an estimated cost benefit of around 20% and simplifies the process. The value is not limited to eliminating one lithography exposure. It also removes associated process steps, reduces overlay complexity and lowers the number of defect opportunities. This is why the correct economic comparison is not one HNA exposure versus two LNA exposures, but one HNA exposure versus the full LNA multi patterning flow.

- **P19 Local Interconnects: The Strongest Logic Cost Case.** The P19 use case is the most compelling near term logic example. A local interconnect layer that requires 3 LNA exposures can be printed with a single HNA exposure. This is consistent with our HNA cost analysis, which takes into account only lithography costs and indicates that triple-patterning LNA is already more expensive than HNA SE in 2026. **ASML estimated cost benefit of around 35% and significantly reduces process complexity.** The tighter the pitch, the more valuable this becomes, because the LNA alternative requires more mask splits and more litho etch loops. This is the type of critical layer where HNA should be inserted first in logic, because the cost and complexity of staying on LNA become increasingly unattractive (Exhibit 39).

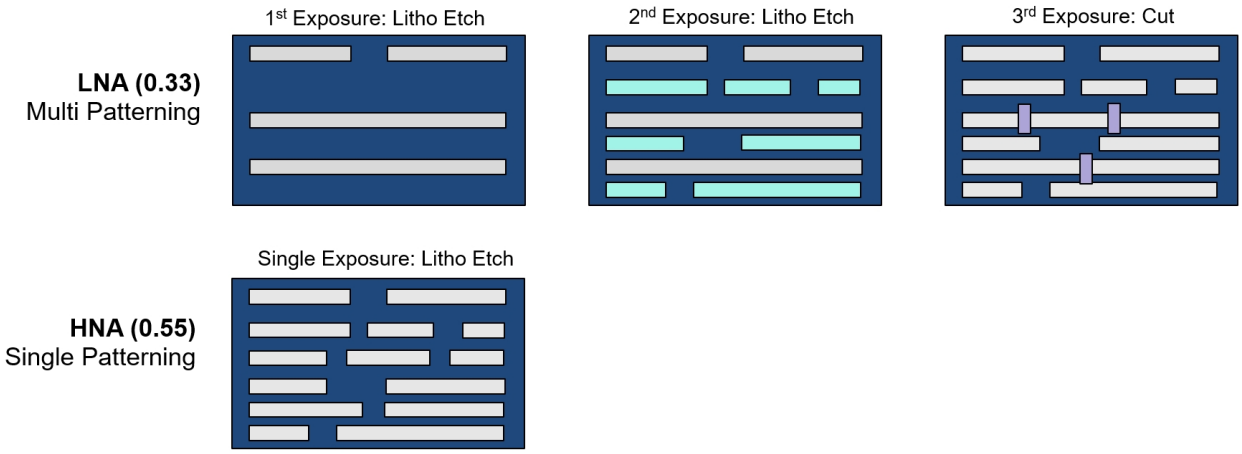
EXHIBIT 38: **In logic P36, HNA delivers sharper pupil-enabled imaging and higher contrast, cutting dose from 250 to 77 mJ/cm² while lifting throughput from 52 to 136 wafers/hour and improving contact-hole quality versus LNA.**



Source: Company reports, Bernstein analysis

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EXHIBIT 39: **P19 highlights the strongest near-term case for HNA in logic, replacing 3 LNA exposures with one, reducing lithography cost by ~35%, simplifying processing, and delivering greater value at tighter pitches where LNA complexity and costs escalate.**



Source: Company reports, Bernstein analysis

Extending Logic Metal Toward 18nm Pitch

Recent HNA results also show extendibility toward 18nm logic metal pitch. The latest logic metal data show T2T CD of 14.6nm, LCDU of 3.6nm at 82 mJ/cm² and more than 48nm visual depth of focus, with MOR resist, mask and pupil optimization still ongoing toward a 3.0nm LCDU target. This supports the view that HNA can extend single exposure metal patterning as future logic nodes tighten. IMEC estimates HNA could be used until 14-18nm metal pitch.

Enabling Two Dimensional Logic Design

HNA also changes what designers can do. With LNA multi patterning, designers are often pushed into restrictive one dimensional routing schemes, where metal lines run in one direction and additional via or metal layers are needed to connect structures. HNA enables more flexible 2D layouts. This can improve routing efficiency, shrink logic cells and potentially reduce the total number of metal layers. The technology has shown reduced and simpler design rules, including bidirectional routing at around 22 to 24nm pitch in one direction and 40 to 44nm pitch in the other. This makes HNA a design scaling tool, not just a lithography productivity tool (Exhibit 40).

The Half Field Challenge for Large Logic Die

As we've already mentioned, the main challenge for logic is the HNA half field. Unlike DRAM, where many dies are small enough to fit inside a half field, advanced logic dies can be much larger, especially for CPUs and GPUs. Large die may therefore need to be split across two half fields and stitched together. Stitching requires careful control of overlay, CD continuity and routing across the boundary. However, block and route stitching solutions are now available, using overlap regions between two 16.5mm half field exposures to enable full field chip designs. This does not remove the complexity, but it makes large die HNA insertion increasingly practical.

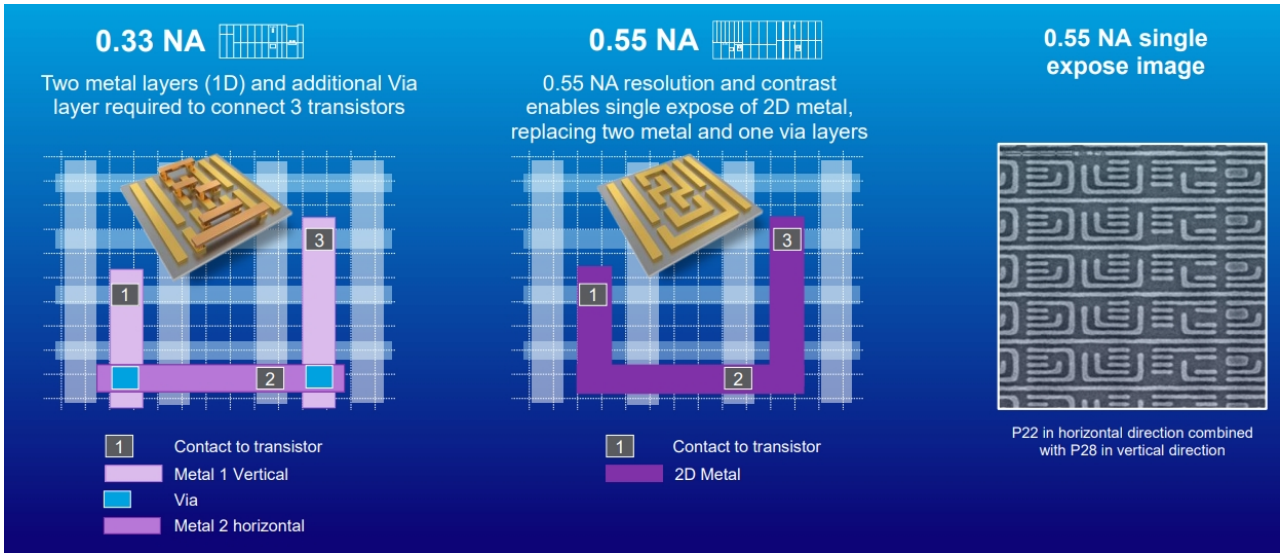
Adoption and Cost Roadmap

Intel has just disclosed that it adopted HNA for selected Intel 18A layers, marking the first high-volume logic production use case and demonstrating that HNA is ready for manufacturing insertion. However, broader logic adoption is still expected to occur around A14, where more HNA exposures are likely to be used on critical layers. The cost roadmap shows HNA becoming cost affordable at A14 for critical logic layers, with improvement from around 18% at HVM A14 to ~24% with future extendibility. By 2030, advanced logic is expected to use around 25 to 30 total EUV exposures, including around exposures on average. The adoption rationale is clear: HNA reduces mask splits, simplifies process flows, impro enables more flexible design rules and keeps critical logic scaling economically viable (Exhibit 41).

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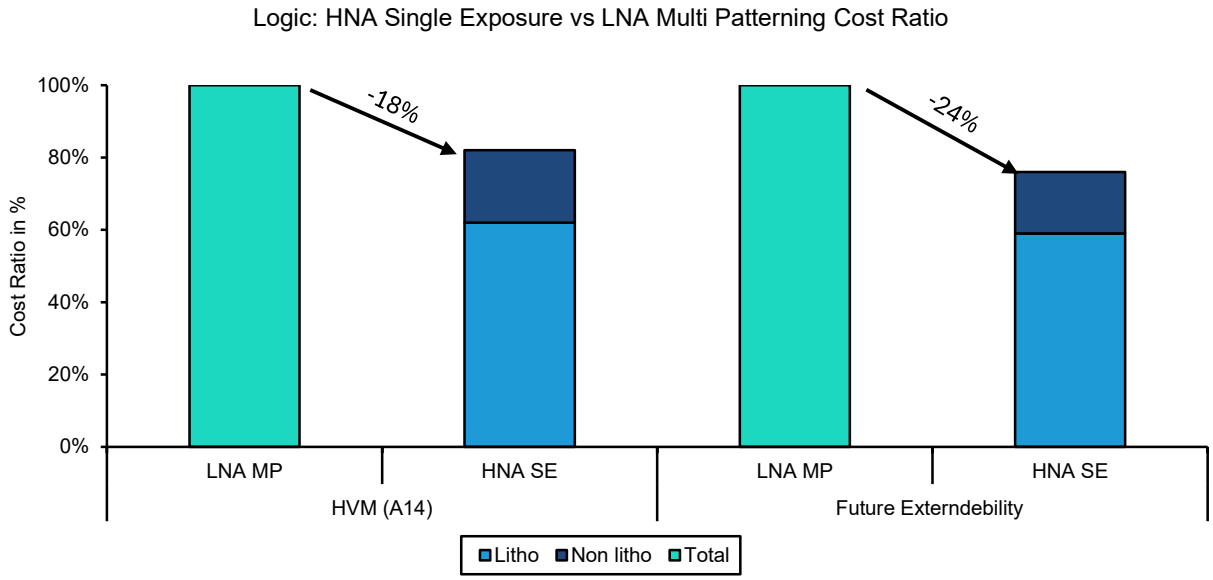
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EXHIBIT 40: **HNA enables single exposure 2D metal routing, replacing LNA multi layer interconnect schemes and reducing metal and via complexity while improving logic cell density and routing flexibility**



Source: ASML

EXHIBIT 41: **HNA reduces logic patterning cost versus LNA by 18% at A14 HVM and 24% with future extendibility, driven by lower litho and even lower non litho costs as single exposure HNA simplifies process complexity**



Source: Company reports, Bernstein analysis

DRAM EMERGES AS THE LIKELY FIRST HNA ADOPTER

The Patterning Challenge at Advanced DRAM Nodes

DRAM chips are built around arrays of capacitors and transistors, connected through tiny cylindrical holes called contact holes. As DRAM generations advance, these holes must be packed closer together, with the most critical layers now targeting pitches of 28 to 32nm. The pitch is the centre-to-centre distance between adjacent holes. At these dimensions, LNA can no longer print these patterns in a single exposure. For a critical DRAM capacitor layer at 15nm contact holes, the current approach requires three separate exposures: two LNA EUV steps and one DUV step, each followed by its own etch and trim process. This

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multi-patterning approach dramatically increases process complexity, cycle time, and fab floor space consumption, and each additional mask step introduces new sources of defects and yield loss.

Why Higher Contrast Changes Everything

The fundamental technical advantage of High-NA EUV, with its numerical aperture of 0.55, comes from higher resolution and stronger contrast. A higher NA captures a larger cone of diffracted light from the mask, producing a sharper, higher-contrast aerial image at the wafer surface. Better contrast leads to lower dose, lower dose leads to higher productivity, higher productivity leads to better cost. ASML quantifies this improvement as a 40% improvement in LCDU (Local Critical Dimension Uniformity) over LNA, which translates into a 1.4x times reduction in pattern variability at 1.4x times lower dose. LCDU improvement is critical in DRAM.

LCDU and Dose: HNA single exposure provides 50% cost benefit vs. LNA

LCDU is the measure of how consistently each contact hole is sized across the array. In a DRAM chip containing billions of holes, a contact hole even 2nm too wide risks shorting to an adjacent cell, while one too narrow creates excess resistance and a failed bit. On DRAM contact hole patterns measured across pitches from P40 to P28, High-NA achieves LCDU of 1.4 to 2.3nm at doses of only 45 to 53 mJ/cm².

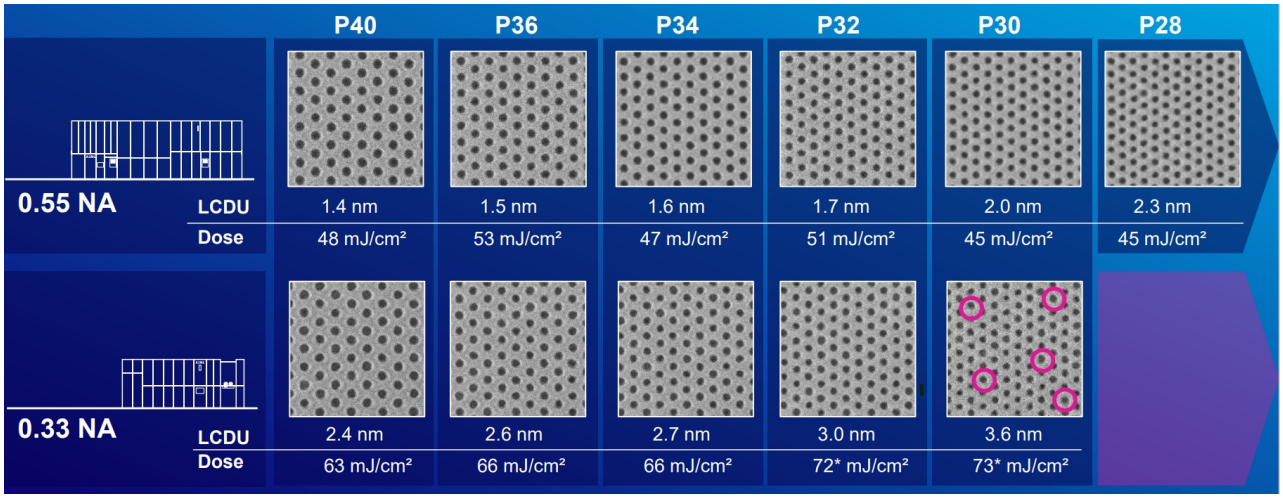
On the same pitch range, LNA, running at practical doses of around 63–73 mJ/cm², delivered significantly worse LCDU of 2.4–3.6 nm. At P30, it also began to show deformed and missing holes, as the lower-contrast aerial image no longer provided a sufficiently clear signal to the resist. ASML explained that, to achieve the same LCDU as HNA, Low NA doses would need to increase to 191–238 mJ/cm². This is theoretical, as these are not doses fabs actually use today, but rather a calculated requirement: the dose Low NA would need if one insisted on pushing its LCDU down to the same 1.4–2.3 nm range that HNA already achieves. Based on this, ASML calculates that, if LCDU is equalised, a HNA single exposure provides around a 50% cost benefit versus LNA exposure, because it achieves the same or better pattern quality with far fewer photons and therefore much higher throughput (Exhibit 42).

The reason is that the LNA aerial image is inherently softer. Photon shot noise has a larger relative impact on the local chemistry, so the only way to reduce that variability is to increase the photon count substantially. In other words, High NA achieves good LCDU almost “for free” through the optics, while Low NA would have to pay for similar LCDU with roughly a 4x increase in dose, which in turn would reduce wafers per hour by a similar factor at a given source power.

In 2026, ASML in collaboration with LAM, demonstrated how far resist engineering can stretch this HNA advantage. By optimising a chemically amplified resist on HNA, the partners reported 1.5 nm LCDU at 87 mJ/cm² with a usable depth of focus of roughly 40 nm across a ±30 nm focus sweep on P28, directly addressing the tighter Depth of Focus (DOF) window that comes with 0.55 NA. A positive tone metal oxide resist (MOR) with dry develop then pushed LCDU further to 1.3 nm at 3σ on 28 nm pitch contact holes, compared to the 2.3nm disclosed in the 2024 Investor day.

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EXHIBIT 42: **Across DRAM contact hole pitches P40–P28, High-NA achieves LCDU of 1.4–2.3 nm at lower doses (45–53 mJ/cm²). Low-NA needs higher doses yet delivers significantly worse overall LCDU, with deformed or missing holes appearing by P30 due to lower image contrast.**



Based on 40nm CAR, *23% illuminator efficiency
Source: ASML

From Triple Exposure to Single Exposure HNA

We believe the process simplification argument is also very compelling. ASML has demonstrated that a DRAM node at 15nm contact holes currently requiring two LNA exposures and one DUV exposure can be replaced by a single HNA exposure, delivering a 30% cost benefit and a significant reduction in process steps, mask count, cycle time, and defect risk. Fewer steps also means less fab floor space dedicated to lithography for the same output volume. Additionally, the HNA exposure produces cleaner, more uniform holes than the triple-exposure Low-NA baseline (Exhibit 43).

The Half-Field Constraint: A Logic Challenge, not a DRAM One

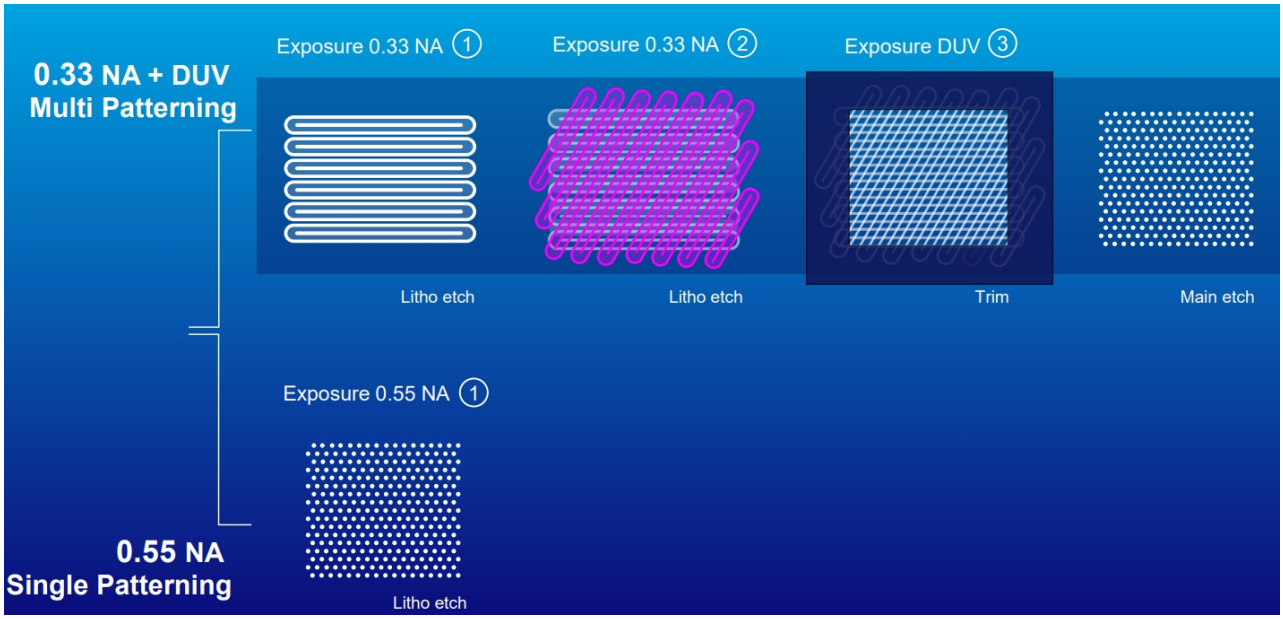
High-NA's anamorphic optics, which use different magnifications in the x and y directions to achieve the higher numerical aperture, reduce the exposure field size to roughly half that of a Low-NA scanner. For DRAM, where individual die are typically small enough to fit within a single half-field, this is manageable: the same mask is simply exposed twice across the full wafer without any stitching complexity. For large logic die that span more than one half-field, a stitching approach is required, where two masks must be precisely aligned at the boundary.

Recent Development and Adoption

Recent ASML commentary suggests that DRAM customers are making solid progress in qualifying HNA EUV in R&D. The key near-term focus remains qualification and product-wafer testing, with insertion decisions and follow-on orders more likely to materialize in 2H26 and into 2027. ASML's Investor Day model assumes that DRAM EUV intensity roughly doubles from around 5 EUV exposures in 2025 to 7–10 EUV exposures by 2030, with 2–3 of those exposures, on average, expected to be HNA. DRAM insertion of High-NA EUV appears positioned around the 0a node, as ASML has described this node as already cost-affordable for critical layers. Specifically, ASML cites a 35% patterning cost reduction versus low-NA EUV in HVM 0a, driven by replacing multi-patterning with a single High-NA exposure and simplifying overall process complexity. We expect it could be even earlier at ~1d. ASML also pushed back on the idea that 4F² DRAM architectures create an EUV demand cliff, arguing that 4F² requires more advanced lithography and should increase both immersion and EUV intensity (Exhibit 44).

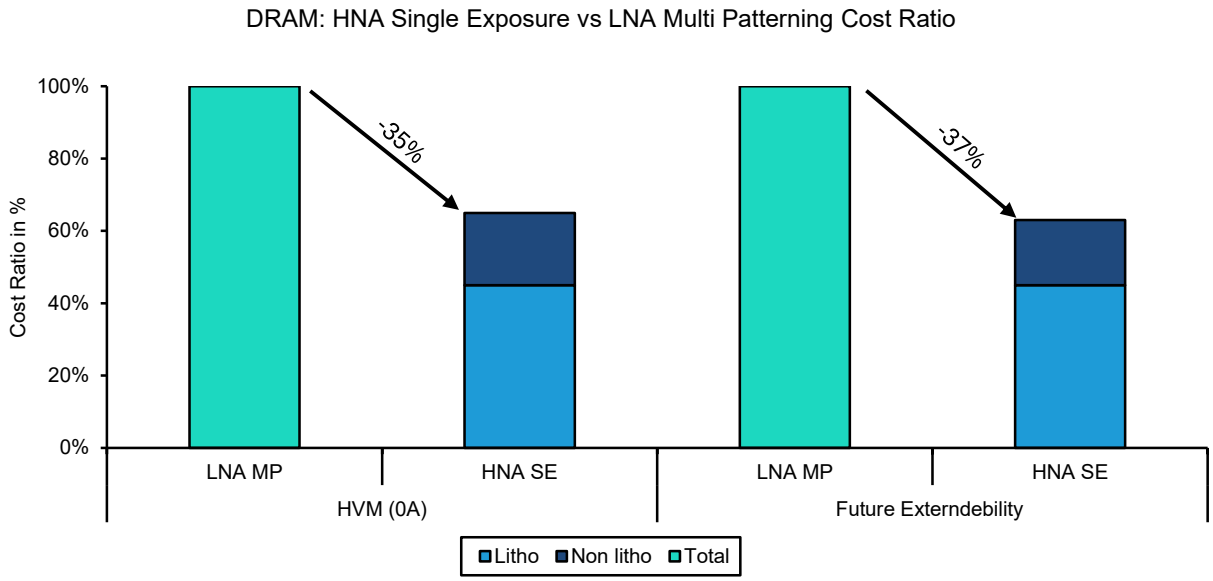
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EXHIBIT 43: **ASML showed 15nm DRAM contact holes needing 3 exposures can be replaced by one HNA EUV step, cutting costs 30% and reducing steps, masks, time, defects, and fab space, while producing cleaner, more uniform holes than triple-exposure LNA baseline approach.**



Source: ASML

EXHIBIT 44: **HNA reduces cost ratios by 35% at 0A HVM and 37% with future extendibility, as both litho and non litho costs decline, with non litho falling faster from lower process complexity and fewer steps overall**



Source: Company reports, Bernstein analysis

NEXT TECH: HYPER NA

Work has already begun on "beyond High-NA" EUV systems

Even before HNA has entered HVM, the next EUV step is already being prepared. This is consistent with how ASML developed HNA itself: HNA R&D began in 2014, several years before LNA EUV reached broad HVM maturity. Hyper NA follows the same

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logic. It is not a committed product yet, but a potential extension of the EUV roadmap that would keep the same 13.5nm wavelength used by LNA and HNA, while increasing numerical aperture toward the 0.75 NA class to support even smaller features.

The likely adoption window is tied less to a fixed calendar date and more to when HNA single exposure no longer provides enough cost effective scaling for the tightest logic interconnect layers. The IMEC roadmap points to continued logic scaling through the angstrom era, with CFET introduction around 2033, and Hyper-NA adoption potentially when the metal pitch scaling eventually approaches the 16nm to 12nm range. That is the range where Hyper NA could become relevant, because HNA is currently positioned to extend logic metal single exposure toward roughly 18nm pitch, but further shrink toward 16nm and then 12nm would likely require either more complex HNA multi patterning or another NA shrink step (Exhibit 45).

The key point is that Hyper NA should be seen as an option embedded in the EUV platform roadmap, not a separate greenfield architecture. The future high productivity common platform is designed to reuse source, stages, interfaces and other common modules across LNA, HNA and potentially Hyper NA, with the main change being the optics. This reduces development risk and gives customers flexibility: Hyper NA can be introduced when logic scaling, likely around CFET and the 16nm to 12nm metal pitch regime, creates a sufficiently strong technical and economic need.

EXHIBIT 45: **IMEC estimates Hyper NA adoption could begin around A3 as metal pitch reaches 12 to 16nm, extending EUV scaling beyond HNA for Logic**



Source: IMEC

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ASML Holding NV

For ASML, we apply a 40x P/E multiple to our Q5-8 EPS estimate to get a rounded PT of €2,500. For the ASML US listing we apply the EUR/US$ exchange rate to get to a rounded PT of USD 2,859.

RISKS

ASML Holding NV

Downside risks to our price target for ASML include margins coming below expectation because of the higher cost to commercialise EUV and advance EUV to new generations, larger than expected China over-stocking, weaker than expected WFE market, slower technology migration and the threat from other technologies in the long run, and further tightened export control on China customers.

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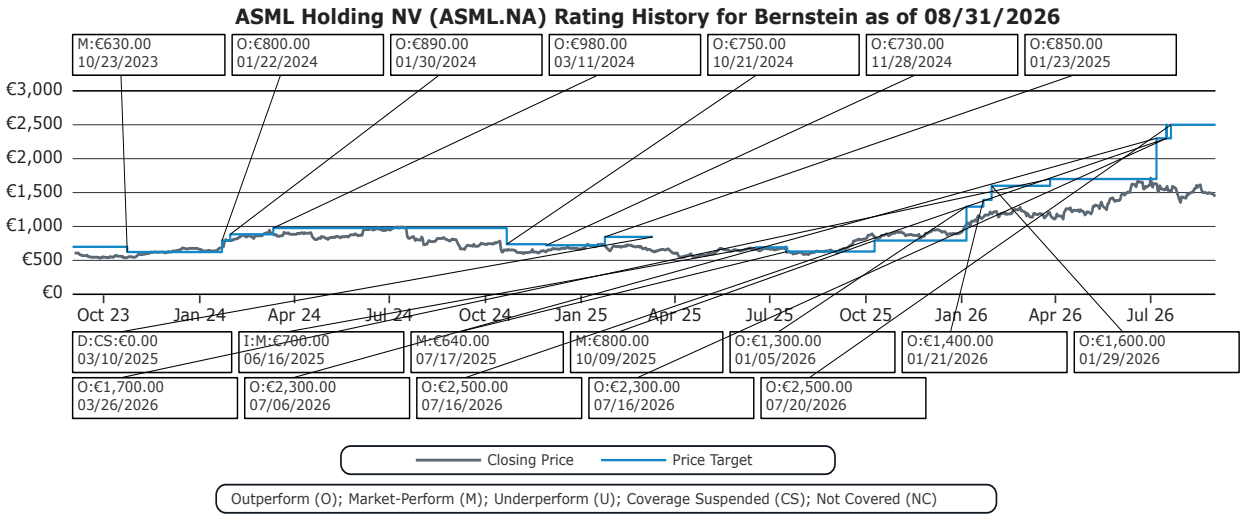
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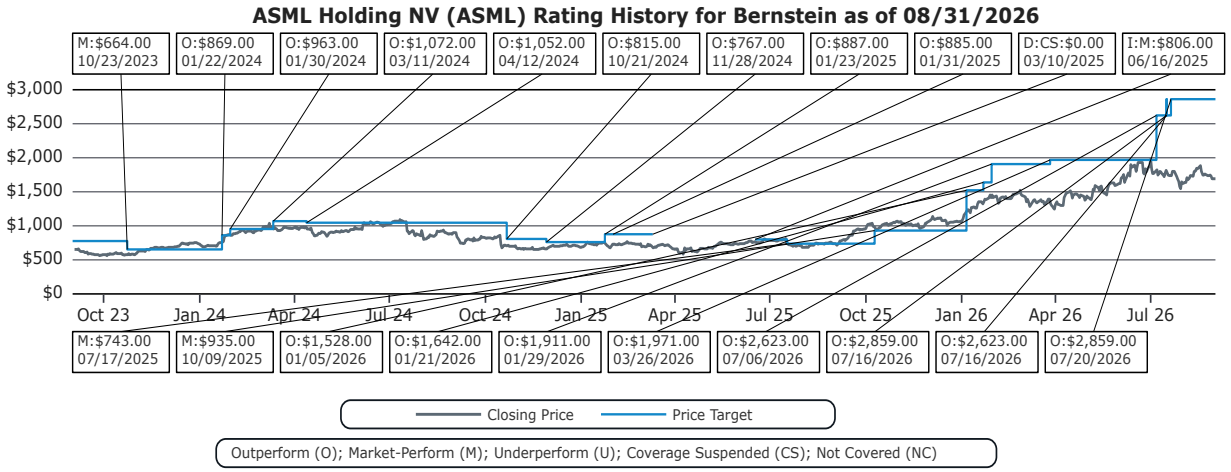
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