BERNSTEIN
SOCIETE GENERALE GROUP

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Japan/EU Semis and Global Memory

Besi, DISCO & Global Memory – Push out of HBM hybrid bonding is likely temporary



David Dai, CFA
+852 2918 5704
david.dai@bernsteinsg.com



Mark Li
+852 2123 2645
mark.li@bernsteinsg.com



Juho Hwang
+81 3 6777 6980
juho.hwang@bernsteinsg.com



Carmine Milano, CFA
+44 20 7762 1857
carmine.milano@bernsteinsg.com



Edward Hou, CFA
+852 2123 2623
edward.hou@bernsteinsg.com

Hybrid Bonding (HB) adoption in HBM is likely to be delayed as we've flagged. As mentioned in our previous report on Besi, we highlighted some downside from the expectation of 2027 adoption of hybrid bonding, expecting the adoption to be more for HBM5 in 2028. More recently, a news report suggested that the industry is now focusing on 8-hi instead of 12-hi for at least HBM4, and even for HBM4E, & 8-hi seems more likely to be the mainstream — which pushes 16-hi and the accompanying hybrid adoption out further away. There are several reasons behind the move: 1. Supply constraint and customers need to spread memory over more XPUs; 2. It seems like some suppliers are facing challenges in 12-hi shipment; 3. High memory cost. In short, the conclusion is that HB is unlikely to see a broad-based adoption in memory within 2027, consistent with our previous view.

HB is still needed eventually. In the recent hot chips conference, SK hynix presented the latest view on HBM packaging, which highlights the benefits of hybrid bonding such as more memory capacity, higher performance and more thermal efficiency. It also labeled "Hybrid Bonding" next to Adv. MUF for 16-hi, suggesting the possibility of adoption in 2028 as mentioned in our previous report. We expect HBM stack height to resume growth once more supply is available, which drives more adoption of HB.

Logic adoption of HB remains intact. The AI CPU/GPU applications we mentioned in our previous report are all progressing on track. <20% of our forecast for HB demand in 2027 is driven by HBM (which is still possible given advanced capacity build out and equipment pull in), suggesting the majority of HB demand is unchanged by the recent HBM development. In 2028, we forecast 36% of HB demand will be from HBM, assuming a modest 10% penetration, which is still plausible.

Impact on Besi / DISCO likely not permanent. Although a push-out for hybrid bonding adoption in HBM seems likely, long-term technological trend towards HB does not change. For Besi, many other drivers such as logic hybrid bonding and conventional packaging is unchanged. Even though management has been communicating in favor of potential HB adoption in HBM as early as HBM4, the market probably would not have been baking this scenario in too seriously, in our view. For Disco, as the overall DRAM wafer consumption itself remains strong, and likewise for dicing / grinding demand, regardless of whether it's for HBM or conventional. Other new drivers such as NAND W2W bonding, BSPDN, and potential upside from SiPh should continue to support Disco's growth.

De-spec'ing is likely, but it does not affect our investment thesis on memory stocks. We believe memory capacity is the predominant reason and memory supply will stay short for 2027. Depending on AI demand then, memory may normalize in 2028, but we model margins exiting 2028 to be still very healthy. With a recent correction, we maintain Outperform on Samsung, SK hynix & Micron, but Underperform on KIOXIA on long-term threat from China.

See the Disclosure Appendix of this report for required disclosures, analyst certifications and other important information. Alternatively, visit our Global Research Disclosure Website.

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BERNSTEIN TICKER TABLE

			2 Sep 2026		TTM	Reported EPS			Reported P/E (x)		
Ticker	Rating	Cur	Closing Price	Price Target	Rel. Perf.	Cur	2025A	2026E	2027E	2025A	2026E	2027E
BESI.NA (Besi)	O	EUR	192.50	320.00	64.6%	EUR	1.66	4.28	6.60	116.0	45.0	29.1
6146.JP (DISCO)	O	JPY	54,040	99,000	7.2%	JPY	1,245.79	1,830.28	2,336.94	43.4	29.5	23.1
005930.KS (SEC- Samsung)	O	KRW	248,500	440,000	226.3%	KRW	6,611.53	48,393	77,273	37.6	5.1	3.2
005935.KS (SEC-Pref - Samsung)	O	KRW	185,500	374,000	192.1%	KRW	6,611.53	48,393	77,273	28.1	3.8	2.4
SMSN.LI (Samsung)	O	USD	4,636.00	7,350.00	238.4%	USD	116.15	812.39	1,290.80	39.9	5.7	3.6
000660.KS (SK hynix)	O	KRW	1,597,000	3,300,000	477.5%	KRW	60,341	395,677	568,862	26.5	4.0	2.8
MU (Micron)	O	USD	956.08	1,300.00	685.8%	USD	8.29	67.39	158.99	115.4	14.2	6.0
285A.JP (KIOXIA)	U	JPY	51,670	40,000	1840.2%	JPY	1,014.00	10,013	9,656.84	51.0	5.2	5.4
EDME			1,602.47									
JPL			2,650.95									
ASIAX			1,949.13									
EM			1,815.57									
SPX			7,666.60									

O - Outperform, M - Market-Perform, U - Underperform, NR - Not Rated, CS - Coverage Suspended

MU estimate is Adjusted EPS; MU valuation is Adjusted P/E (x);

Source: Bloomberg, Bernstein estimates and analysis.

INVESTMENT IMPLICATIONS

We rate Besi (PT=€320.00), Disco (PT=¥99,000) Outperform.

Samsung Electronics: We rate Samsung Electronics Outperform with price target of KRW 440,000.

SK hynix : We rate SK hynix Outperform with price target of KRW 3,300,000.

Micron: We rate Micron Outperform with price target of US$1,300.00.

KIOXIA: We rate KIOXIA Underperform with price target of JPY 40,000.

DETAILS

Hybrid bonding adoption is likely delayed near term due to HBM de-spec

As mentioned in our previous report on Besi, we highlighted some downside from the expectation of 2027 adoption of hybrid bonding, expecting a broad-based HBM adoption to be more for HBM5 in 2028. More recently, a news report suggested that the industry is now focusing on 8-hi instead of 12-hi for at least HBM4, and even for HBM4E, & 8-hi seems more likely to be the mainstream — which pushes 16-hi and the accompanying hybrid adoption out further away. There are several reasons behind that move: 1. supply constraint and customers need to spread memory over more XPUs; 2. it seems like some suppliers are facing challenges in 12-hi shipment; 3.high memory cost. In short, the conclusion is that HB is unlikely to see a broad-based adoption in memory within 2027, consistent with our previous view.

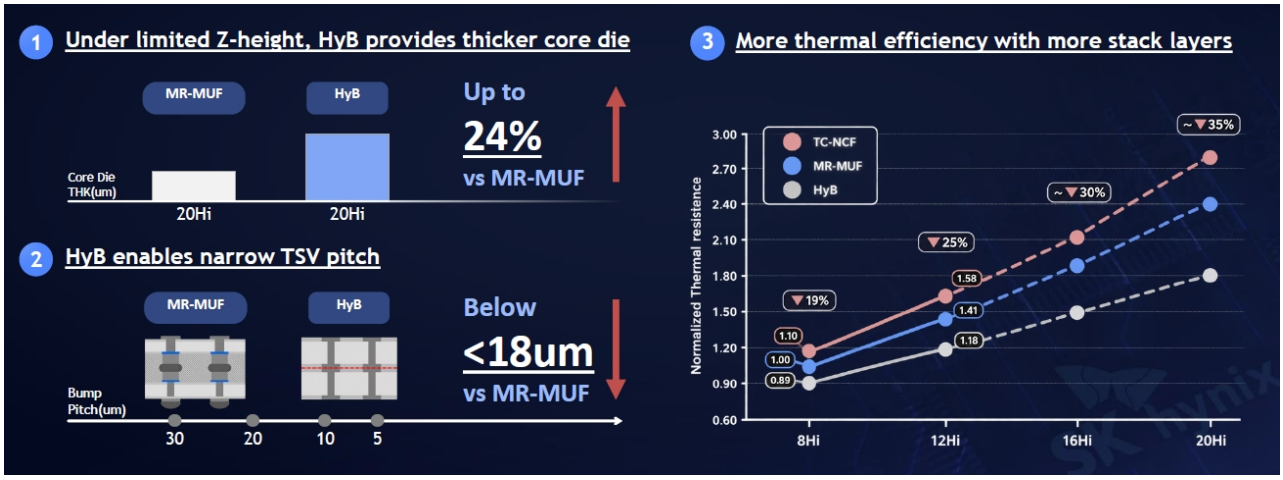
Hybrid bonding is still needed in the longer term

Although, in the recent hot chips conference, SK hynix presented the latest view on HBM packaging (Exhibit 1), which highlights the benefits of hybrid bonding such as more memory capacity, more performance and more thermal efficiency. The rationale to adopt hybrid bonding stems from a structural constraint on HBM stack height. JEDEC caps total package thickness at 775µm so the memory stack stays flush with the adjacent logic die on the interposer, and every additional DRAM layer added within that limit forces each die to get thinner, potentially resulting in low yield due to warpage and heat. SK hynix's pitch for hybrid bonding is that HB addresses these specific issues.

First, by bonding dies directly eliminating microbumps and underfill, hybrid bonding frees up the vertical space that mircrobumps used to occupy, allowing the core dies to be 24% thicker — less prone to warpage-induced yield loss. Second, by removing the need for microbump spacing, TSV / pad pitch can shrink to below 18µm vs. 20-30µm for MR-MUF, allowing for far more interconnects within the same die area, leading to superior bandwidth. Third, because copper-to-copper / oxide-to-oxide interface has much greater thermal conductivity versus the current solder / underfill setup, it improves heat dissipation significantly, which gets compounded and magnified at higher stack counts — resulting in ~35% lower thermal resistance at 20 stacks.

Although worth noting is the fact that JEDEC is reportedly considering to relax HBM height specs to ~900µm, which would give memory makers potentially another generation to stay at the existing MR-MUF / TC-NCF technology, but this is no news and is consistent with our view that the majority of HBM4E will likely not require hybrid bonding, and the three benefits mentioned above remain as the structural argument for a long-term migration towards hybrid bonding.

EXHIBIT 1: **SK hynix highlights more memory capacity, performance and thermal efficiency through hybrid bonding.**

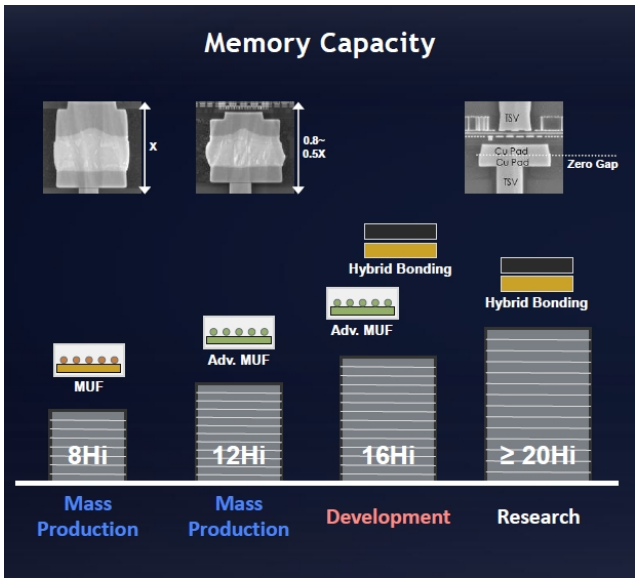


Source: SK hynix, ISMP

We believe the de-spec to 8-hi is only a temporary situation induced by the near term supply constraints. To the extent this supply crunch is resolved and the roadmap returns back to stacking more memory dies, hybrid bonding bonding will have to be adopted. SK hynix seems to expect a partial adoption of hybrid at 16-hi and a full adoption from 20-hi (Exhibit 2), with the main

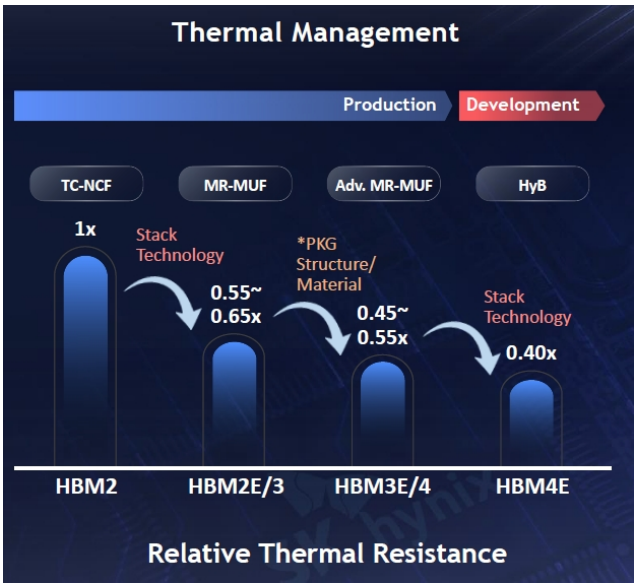
reason / technological constraints that necessitates HB adoption being thermal management (Exhibit 3) among many other reasons.

EXHIBIT 2: **SK hynix's roadmap includes partial hybrid bonding from 16hi, and suggests a full adoption from 20hi.**



Source: SK hynix, ISMP

EXHIBIT 3: **Heat will be the challenge, which hybrid bonding could help alleviate.**



Source: SK hynix, ISMP

OUR FORECAST OF HYBRID BONDING

Bonding technologies are essential to enable advanced packaging — we have written extensively on the different bonding technologies such as Thermocompression bonding (TCB) as well as hybrid bonding (HB) for both High Bandwidth Memory (HBM) and logic applications, in our previous reports (The Bonder War: Part 1 — HBM bonding technology shifts, The Bonder War: Part 2 — Path to advanced packaging for logic chips and The Bonder Primer: Essential enablers of advanced packaging).

This report provides our latest view of the current bonding market as well as an update to our TAM forecast (Exhibit 4). In short,

- We see a clear trend for logic to adopt die-to-wafer (D2W) hybrid bonding to increase interconnection speed between logic chiplets and between logic and memory. For logic, we forecast 2028 HB TAM of $887mn, and 2028 shipment of 237 units (103 prior), to reflect our outlook of stronger adoption at TSMC for SoIC packaging.
- HBM adoption is less clear. While Samsung may adopt HB in HBM4E in 2027, it's possible to be postponed to 2028 with HBM5, with few (maybe 1) initial layer only. We forecast 2028 HB TAM of $489mn, and 2028 shipment of 130 units, based on our view that some portion of HBM4E will adopt hybrid, and HBM5 will migrate to hybrid bonding.
- We forecast the hybrid bonder TAM to surge to c. $1.4bn in 2028, driven by the adoption in both logic and HBM. Compared to Besi's hybrid bonding market forecast, we are more optimistic in logic adoption despite being more conservative with HBM adoption of HB, and our 2028 unit shipment estimates of 367 units is 24% above the mid case and 8% below the high case (Exhibit 5).
- For Besi, assuming 2028 market share of 76% (80% logic, 70% HBM), Besi's revenue from HB would be c. $1.1bn, which is based on unit sales of ~281 units and ASP assumption of $3.75mn per unit.

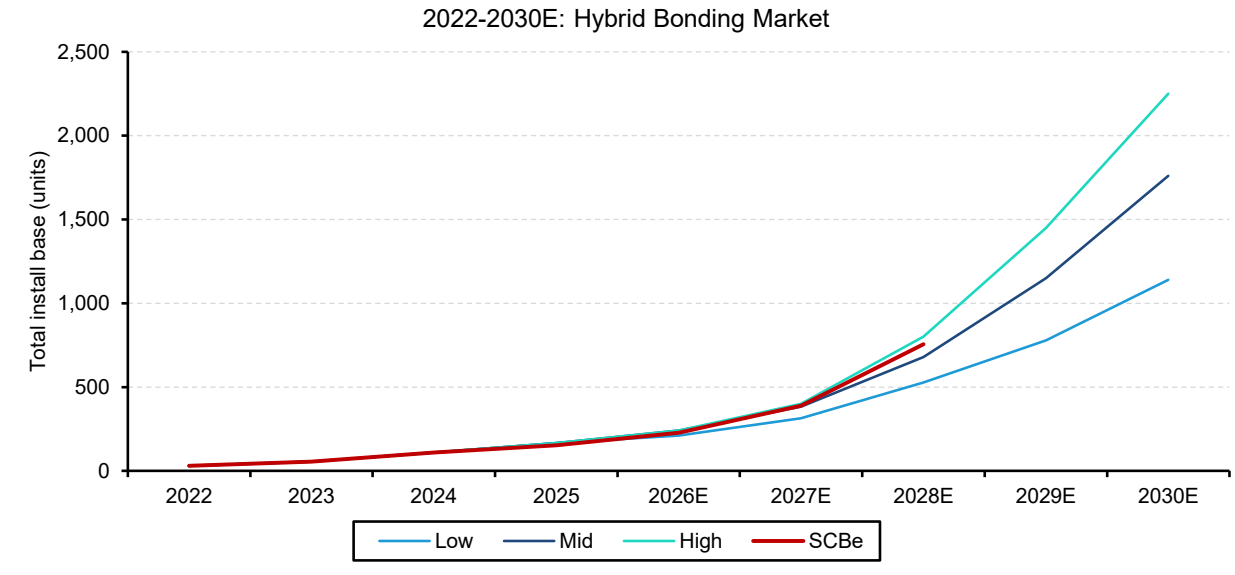
The following sections will discuss logic and HBM adoption in detail.

EXHIBIT 4: **Summary of our TCB / HB market forecast.**

Total Market	2024	2025	2026E	2027E	2028E
TC Bonding TAM	**654.0**	**847.2**	**1,169.7**	**1,601.4**	**2,048.9**
HBM	399.6	478.1	782.3	1,002.5	1,316.0
Logic	254.4	369.1	387.5	598.9	733.0
% YoY		29.5%	38.1%	36.9%	27.9%
Hybrid Bonding TAM	**101.3**	**99.8**	**206.3**	**524.1**	**1,376.0**
HBM	--	--	--	91.8	488.8
Logic	101.3	99.8	206.3	432.4	887.2
% YoY		(1.5%)	106.8%	154.1%	162.5%
Total TCB + HB TAM	**755.2**	**946.9**	**1,376.0**	**2,125.5**	**3,425.0**
HBM	399.6	478.1	782.3	1,094.3	1,804.8
Logic	355.6	468.9	593.7	1,031.3	1,620.2
% YoY		25.4%	45.3%	54.5%	61.1%
Besi HB Revenue	**101.3**	**99.8**	**206.3**	**488.8**	**1,052.0**
HBM	--	--	--	78.0	342.2
Logic	101.3	99.8	206.3	410.8	709.8
Implied Besi Market Share (HB)	**100.0%**	**100.0%**	**100.0%**	**93.2%**	**76.4%**
HBM				85.0%	70.0%
Logic	100.0%	100.0%	100.0%	95.0%	80.0%

Source: Company disclosures, TechInsights, Bernstein estimates and analysis.

EXHIBIT 5: **Our hybrid bonder estimates are between Besi's mid and high case guidance.**



Source: Company disclosures, Bernstein estimates and analysis.

LOGIC: CLEAR TRAJECTORY OF HYBRID ADOPTION

Hybrid bonding is expanding in adoption among the various interconnect technologies, especially for leading-edge chiplet architectures. The key driver remains to be the fact that it enables higher interconnect density while lowering power consumption than with conventional micro-bump based approaches.

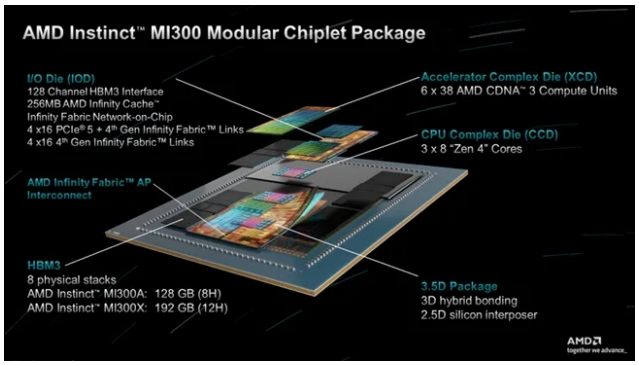
We see three primary use cases for hybrid bonding:

- **XPU-to-XPU chiplet integration (bonding logic on logic):** to improve logic transistor count and boost computing power. Examples of XPU-to-XPU chiplet integrations include AMD's Instinct GPUs (Exhibit 6) utilizing advanced chiplet architectures, as well as future Nvidia multi-die GPU architectures such as Feynman GPUs. Apple's M5 Pro uses unique CPU +GPU chiplet integration named Fusion Architecture.
- **XPU+Memory (bonding memory on logic):** to break the memory wall, and there are a few variations:
  - The most prominent is bonding XPU with SRAM, and AMD's 3D V-Cache architecture (Exhibit 7) is a good example of this, and already with a sizeable production volume. EPYC (Milan-X / Genoa-X) and Ryzen X3D (7800X3D / 9800X3D) series have logic die bonded to cache memory die, to realize improved cache capacity as well as lower latency. The Nvidia Groq LPU is also anticipated to use XPU+SRAM integration in the next generation. Intel is also working on their own architecture of HB named Foveros Direct 3D.
  - There is also XPU bonding with DRAM, as shown in China's LongShine CPU which integrates HBM and DRAM on chip. In the LongShine setup, hybrid bonding helps make DRAM behave more like a first-class extension of the processor package rather than a distant off-package resource.
- **CPO (optical communication):** most prominently TSMC's COUPE which integrates optical chip (PIC) and electrical chip (EIC) together with hybrid bonding (Exhibit 8).

For these applications, we expect **hybrid bonding capacity to increase rapidly**, leading to strong growth of hybrid bonding equipment revenue. In terms of capacity, TSMC and Intel are the leaders.

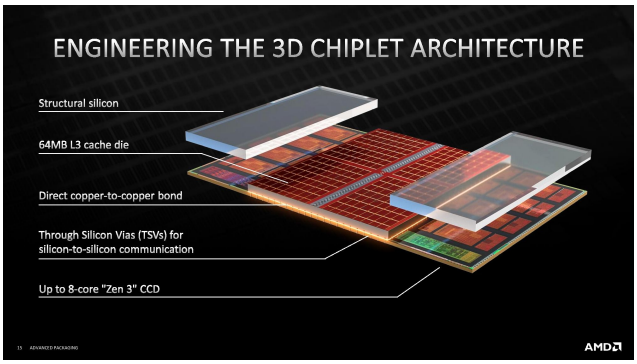
- For TSMC (covered by Mark Li), current use cases are mainly for AMD CPUs and GPUs mentioned above, and some for Apple (M5 Pro / M5 Max). Going forward, we expect TSMC's HB capacity to nearly double for both this year and next year driven by increased adoption, for Broadcom's 3.5D packaging as well as for Nvidia's Feynman GPUs.
- Intel (covered by Stacy Rasgon) has already deployed hybrid-bonding based architectures through their Foveros Direct 3D platform and remains strategically committed to advanced 3D packaging. Intel's Clearwater Forest is an instance of their HB adoption, and we expect higher adoption going forward as Diamond Rapids and subsequent CPUs start ramping. As for Intel, we don't anticipate much ramp in HB capacity quite yet in 2026 as they already have 30 units of hybrid bonders, and Diamond Rapids seems to be delayed to 2027, but capacity expansion should happen again from 2027 (Exhibit 9-Exhibit 11).

EXHIBIT 6: **AMD Instinct GPUs employing XPU-XPU chiplet integration**



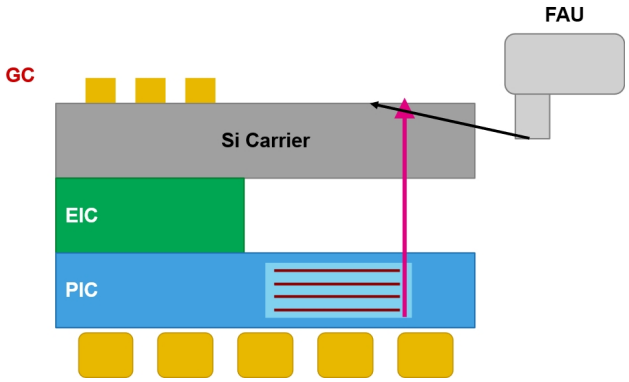
Source: AMD

EXHIBIT 7: **AMD 3D V-cache employing XPU-Memory bonding**



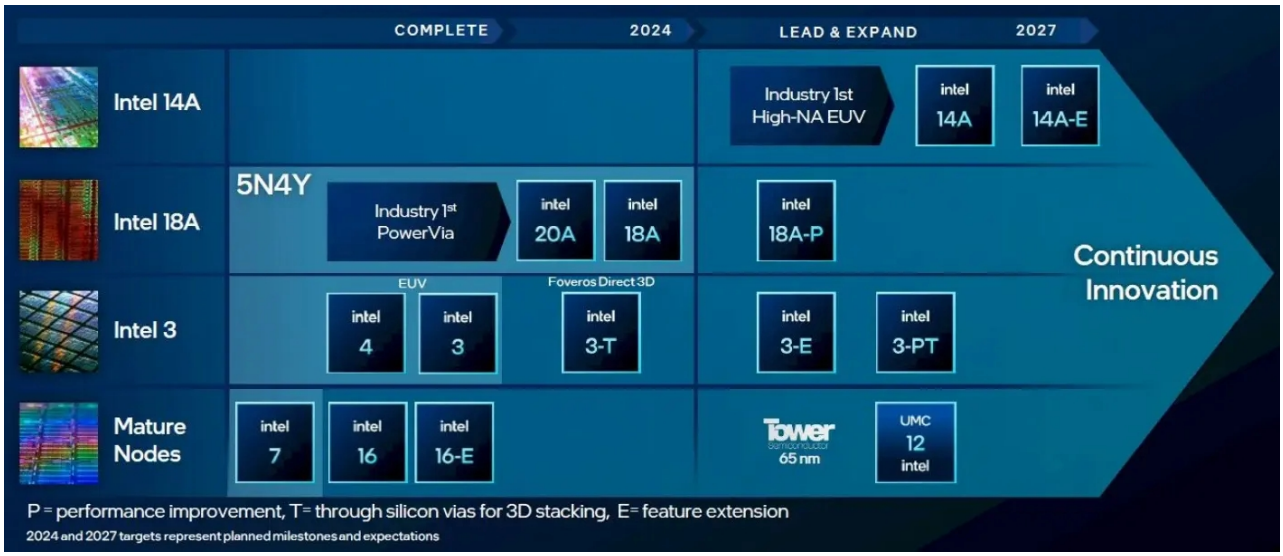
Source: AMD

EXHIBIT 8: **Optical interconnects employing hybrid bonding.**



Source: Bernstein analysis.

EXHIBIT 9: **Intel product roadmap with Foveros Direct 3D**



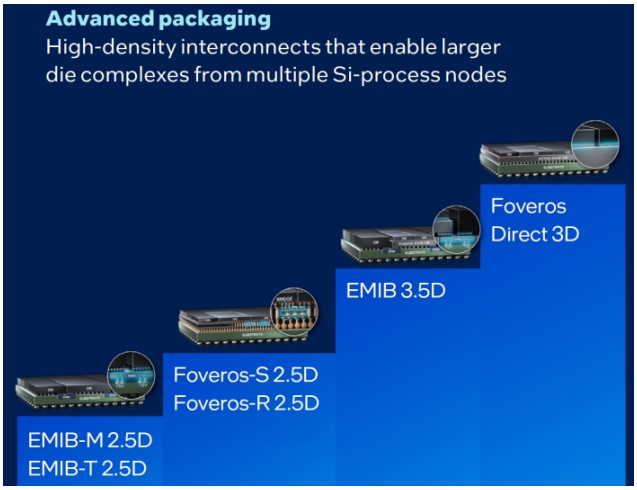
Source: Intel

EXHIBIT 10: **Intel Clearwater Forest is Intel's first major CPU that employs hybrid bonding to connect CPU chiplet to base chiplet, before bonding to EMIB substrate.**



Source: Intel

EXHIBIT 11: **Hybrid bonding (Foveros Direct 3D) is a key technology to enable Intel's product roadmap.**

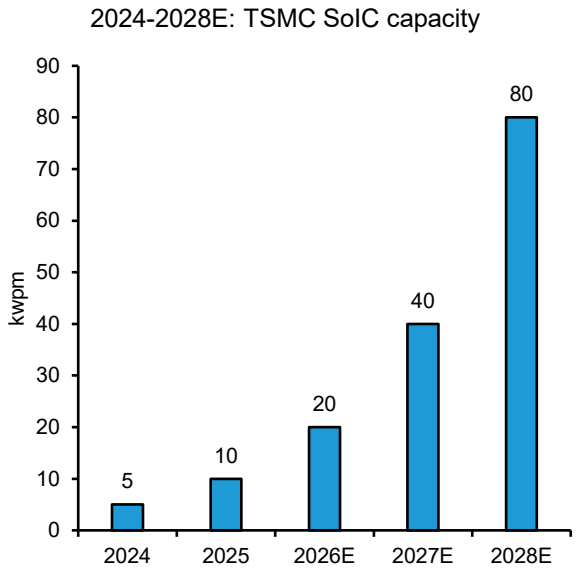


Source: Intel

In terms of TAM, we expect a strong ramp and model the **logic hybrid bonding capacity (installed base) to grow 4.5x to 582 units in 2028 from 137 units in 2025** (Exhibit 13).

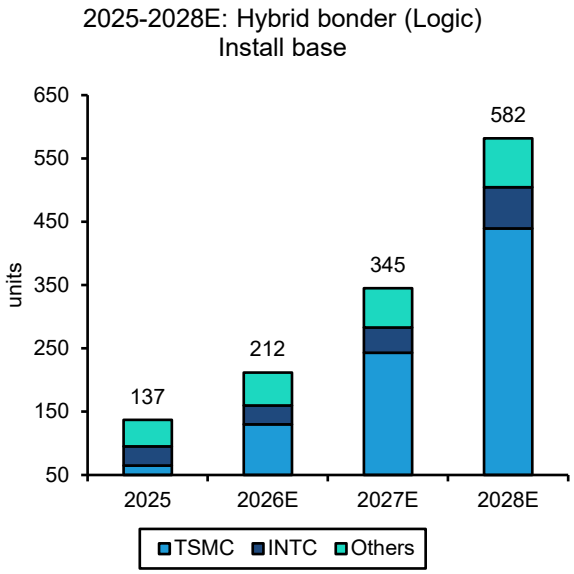
- We believe the install base at TSMC could reach ~440 units as AP7 followed by AP8 ramps up — from the current ~65 unit fleet mostly in AP6. AP7 capacity expansion occurring in three phases: 1. Initial SoIC applications 2. HPC chiplet deployment 3. More broad-based adoption such as wafer-level multi-chip module (WMCM) adoption.
- We expect TSMC's capacity grow ~8x from 10kwpm in end 2025 to 80kwpm in 2028 (Exhibit 12), driven by the adoption of AMD, Apple, followed by Google TPU, Groq LPU, and Nvidia GPU (Feynman).
- At a higher level, we estimate that each kwpm SoIC capacity addition requires around 5-6 hybrid bonders, and that the intensity will go down over time as hybrid bonding throughput improves.
- For Intel, we expect them to resume HB capacity addition from 2027 and model the install base to reach ~65 units in 2028 from the current install base of ~30 units, and others (including Samsung) doubling to ~68 units from ~33 units. As a result, we expect the logic HB TAM to reach $887mn in 2028, effectively growing eightfold from 2025 (Exhibit 14).

EXHIBIT 12: **We expect TSMC's capacity to grow rapidly to 80kwpm in 2028.**



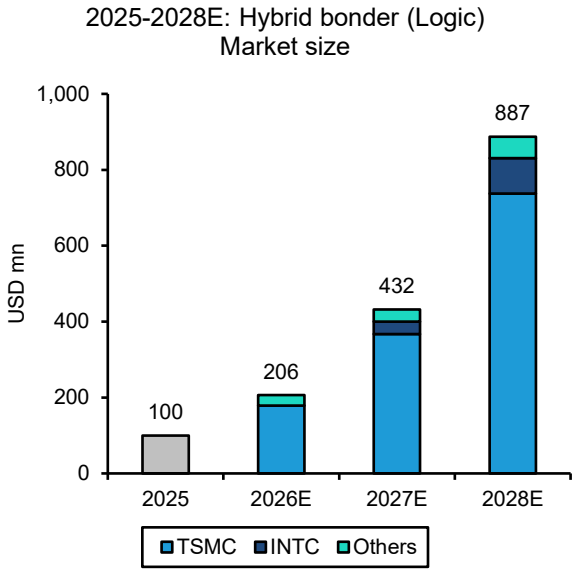
Source: Company disclosures, Bernstein estimates and analysis.

EXHIBIT 13: **We expect the install base to grow 4.5x in 3 years.**



Source: Company disclosures, Bernstein estimates and analysis.

EXHIBIT 14: **As a result, we expect logic hybrid bonder TAM to reach $887mn in 2028.**



Source: Company disclosures, TechInsights, Bernstein estimates and analysis.

HBM: UNCERTAINTIES STILL PRESENT IN HB PENETRATION

While hybrid bonding has become increasingly established in logic applications, adoption within HBM is likely to proceed more gradually. The primary reason is that the current TCB solutions remain highly effective and sufficient for many HBM requirements, especially given that 1. JEDEC seems increasingly likely to relax HBM height standards to ~900µm from the current 775µm, 2. HBM4E seems likely to stay mostly at 8/12-hi. Both Samsung and SK Hynix are coming up with new ways to better dissipate heat.

However, in the longer term, we believe factors such as increasing number of layers to stack as well as increase in I/O channels to 4,096 from the current 2,048 eventually would create an incentive to migrate selected layers (Exhibit 15) toward hybrid bonding. We view Samsung to lead the HB adoption followed by SK hynix and Micron, although we believe the majority will continue to be TCB up to 2028. In terms of new capacity addition, we believe TCB shipment should drop after 2028.

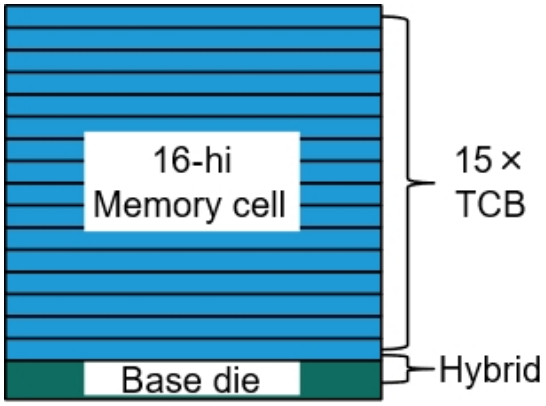
Below are our current expectations and potential changes/risks in HBM adoption of HB:

- It looks likely that Samsung could start adoption of HB from 2028 with 16-hi HBM5, and HBM4E would likely stay at 8/12-hi.
- Hynix and Micron are also likely to start adoption in 2028 for HBM5. We expect that TCB will still be mainstream technology by then, but TCB shipment will start to decline in 2028 while HB increases steadily.

Below is our current estimates of TCB / hybrid bonding for HBM, although we have not changed our estimates at this time.

- As HBM is easier and has lower alignment accuracy requirement, it should be much faster than logic. Every kwpm HBM bonding capacity would only require ~2-3 bonders, less than half of that for logic. Assuming 15% blended penetration in total 1,202kwpm HBM capacity, we derive the HB revenue for HBM bonding to be $489mn and $1.8bn in total combined with TCB (Exhibit 17).
- Adding HBM and logic demand, we get total HB TAM of $1.4bn in 2028 (Exhibit 18).

EXHIBIT 15: **Even in case of HB adoption in 16-hi HBM4E, we believe the adoption would be limited to just 1 layer.**



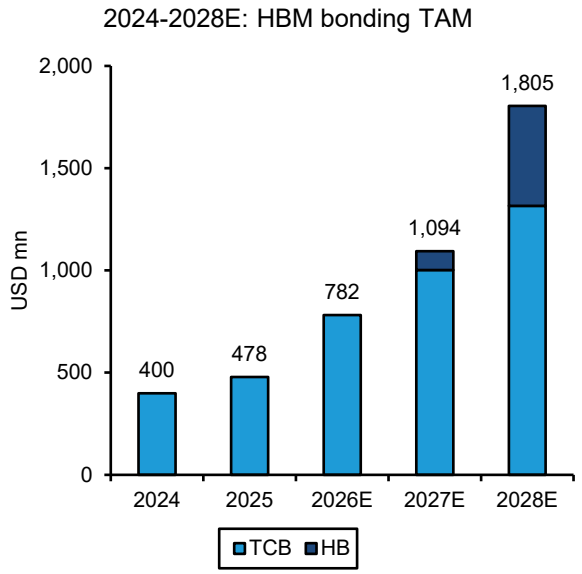
Source: Bernstein analysis.

EXHIBIT 16: **HBM bonding technology roadmap.**

Vendor	HBM4E	HBM5
SAMSUNG	8/**12**/16-hi (TCB)	12-hi (TCB) / 16-hi (HB+TCB)
SK hynix	8/**12**/16-hi (TCB)	12-hi (TCB) / 16-hi (TCB)
micron	8/**12**/16-hi (TCB)	12-hi (TCB) / 16-hi (HB+TCB)

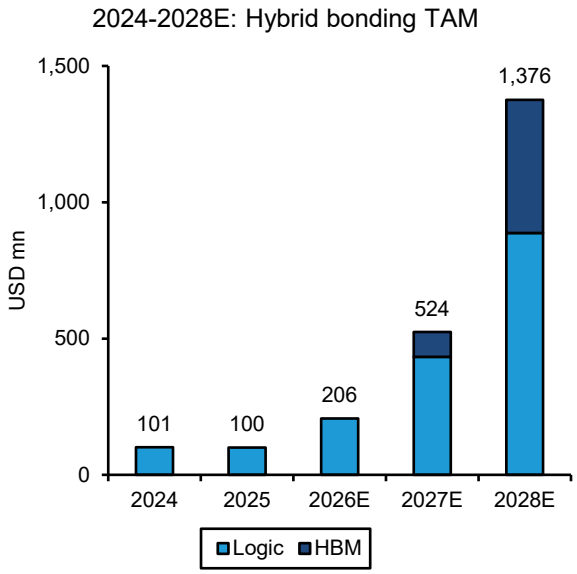
Source: Bernstein estimates and analysis.

EXHIBIT 17: **We expect strong HBM bonding growth up to 2028, reaching $1.8bn.**



Source: TechInsights, Bernstein estimates and analysis.

EXHIBIT 18: **We estimate 2028 HB TAM of $1.4bn of which 36% is HBM.**



Source: Company disclosures, TechInsights, Bernstein estimates and analysis.

I. REQUIRED DISCLOSURES

References to "Bernstein" or the “Firm” in these disclosures relate to the following entities: Bernstein Institutional Services LLC (April 1, 2024 onwards), Sanford C. Bernstein & Co., LLC (pre April 1, 2024), Bernstein Autonomous LLP, BSG France S.A. (April 1, 2024 onwards), Sanford C. Bernstein (Hong Kong) Limited 盛博香港有限公司, Sanford C. Bernstein (Canada) Limited, Sanford C. Bernstein (India) Private Limited (SEBI registration no. INH000006378), Sanford C. Bernstein (Singapore) Private Limited, Sanford C. Bernstein Japan KK（サンフォード・C・バーンスタイン株式会社）and analysts employed by Société Générale Africa Technologies & Services to produce Bernstein research under a Global Services Agreement in place between Bernstein and Société Générale.

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VALUATION METHODOLOGY

BE Semiconductor Industries NV

For Besi, we set a €320 price target using a P/E multiple of 40x against our forward Q5-Q8 EPS estimate.

Disco Corp

We set a price target of ¥99,000 using a P/E multiple of 40x against our forward Q5-Q8 EPS estimate.

Samsung Electronics Co Ltd

We value Samsung Electronics with 6.2x of forward 5Q-8Q EPS of KRW71,172 and arrive at price target of KRW 440,000 for its common shares, KRW374,000 for preferred shares, and US$7,350 for GDR.

SK Hynix Inc

We value SK hynix with 6.2x of forward 5Q-8Q EPS of KRW536,158 and arrive at price target of KRW3,300,000.

Micron Technology Inc

We value Micron with 7.7x of forward 5Q-8Q EPS of US$169.8 and arrive at price target of US$1,300.

KIOXIA Holdings Corp

We value KIOXIA with 4.1x of 1-year forward EPS of ¥9,810 and arrive at price target of ¥40,000.

RISKS

BE Semiconductor Industries NV

Downside risks to our price target for Besi include short-term — lower than expected or delayed adoption of hybrid bonding and a prolonged delay in the recovery of the mainstream assembly market — losing market share in hybrid bonding or lack of take-up of Besi’s TCB offering.

Disco Corp

There are a number of downside risks to our DISCO target price: (1) Overcapacity of AI-related production such as GPUs and HBM resulting in both multiple contraction and earning power (2) Changes in competitive environment (3) Unfavorable exchange rate fluctuation with downside risk to its revenue.

Samsung Electronics Co Ltd

The biggest downside risk to our target price is an earlier end of favorable pricing environment, which can be a result of weaker demand or higher supply. Investor sentiment and hence the valuation rewarded by investors is also a risk. China's progress in

memory, especially in NAND, is a downside risk too.

SK Hynix Inc

The biggest downside risk to our target price is an earlier end of favorable pricing environment, which can be a result of weaker demand or higher supply. Investor sentiment and hence the valuation rewarded by investors is also a risk. China's progress in memory, especially in NAND, is a downside risk too.

Micron Technology Inc

The biggest downside risk to our target price is an earlier end of favorable pricing environment, which can be a result of weaker demand or higher supply. Investor sentiment and hence the valuation rewarded by investors is also a risk. China's progress in memory, especially in NAND, is a downside risk too.

KIOXIA Holdings Corp

Upside risk to our target price include 1) stronger than expected NAND demand growth, which likely would lead to better NAND pricing and hence company earnings, 2) favorable policy support from Japanese government such as capex subsidies, and 3) better than expected cost reduction

RATINGS DEFINITIONS, BENCHMARKS AND DISTRIBUTION

EQUITY RATINGS DEFINITIONS

Bernstein brand

The Bernstein brand rates stocks based on forecasts of relative performance for the next 12 months versus the S&P 500 for stocks listed on the U.S. and Canadian exchanges, versus the Bloomberg Europe Developed Markets Large and Mid Cap Price Return Index EUR (EDME) for stocks listed on the European exchanges and emerging markets exchanges outside of the Asia Pacific region, versus the Bloomberg Japan Large and Mid Cap Price Return Index USD (JPL) for stocks listed on the Japanese exchanges, and versus the Bloomberg Asia ex-Japan Large and Mid Cap Price Return Index (ASIAX) for stocks listed on the Asian (ex-Japan) exchanges -unless otherwise specified.

The Bernstein brand has three categories of ratings:

- Outperform: Stock will outpace the market index by more than 15 pp
- Market-Perform: Stock will perform in line with the market index to within +/-15 pp
- Underperform: Stock will trail the performance of the market index by more than 15 pp

Coverage Suspended: Coverage of a company under the Bernstein research brand has been suspended. Ratings and price targets are suspended temporarily, are no longer current, and should therefore not be relied upon.

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Not Covered (NC) denotes companies that are not under coverage.

Bernstein brand stock ratings are based on a 12-month time horizon.

Autonomous brand – common stocks

The Autonomous brand rates common stocks as indicated below. As our benchmarks we use the Bloomberg Europe 600 Financials Price Return Index (E600BK) and Bloomberg Europe Dev Mkt Financials Large and Mid Cap Price Ret Index EUR (EDMFI) index for developed European banks and Payments, the Bloomberg Europe 600 Insurance Price Return Index (E600IN) for European insurers, the S&P 500 and S&P Financials for US banks and Payments coverage, S5LIFE for US Insurance, the S&P Insurance Select Industry (SPSIINS) for US Non-Life Insurers coverage, the Bloomberg Emerging Markets Financials Large, Mid and Small Cap Price Return Index (EMLSF) for emerging market banks and insurers and Payments, and the Bloomberg Japan Financials Large & Mid Cap Price Return Index (JPFILM) for Japanese Financials. Ratings are stated relative to the sector (not the

market).

The Autonomous brand has three categories of common stock ratings:

- Outperform (OP): Stock will outpace the relevant index by more than 10 pp
- Neutral (N): Stock will perform in line with the market index to within +/-10 pp
- Underperform (UP): Stock will trail the performance of the relevant index by more than 10 pp

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Those denoted as 'Feature' (e.g., Feature Outperform FOP, Feature Under Outperform FUP) are our core ideas.

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- Neutral (N): The total return of the preferred instrument is expected to perform in line with preferred securities of other issuers operating in similar sectors or rating categories over the next six months.
- Underperform (UP): The total return of the preferred instrument is expected to underperform preferred securities of other issuers operating in similar sectors or rating categories over the next six months.

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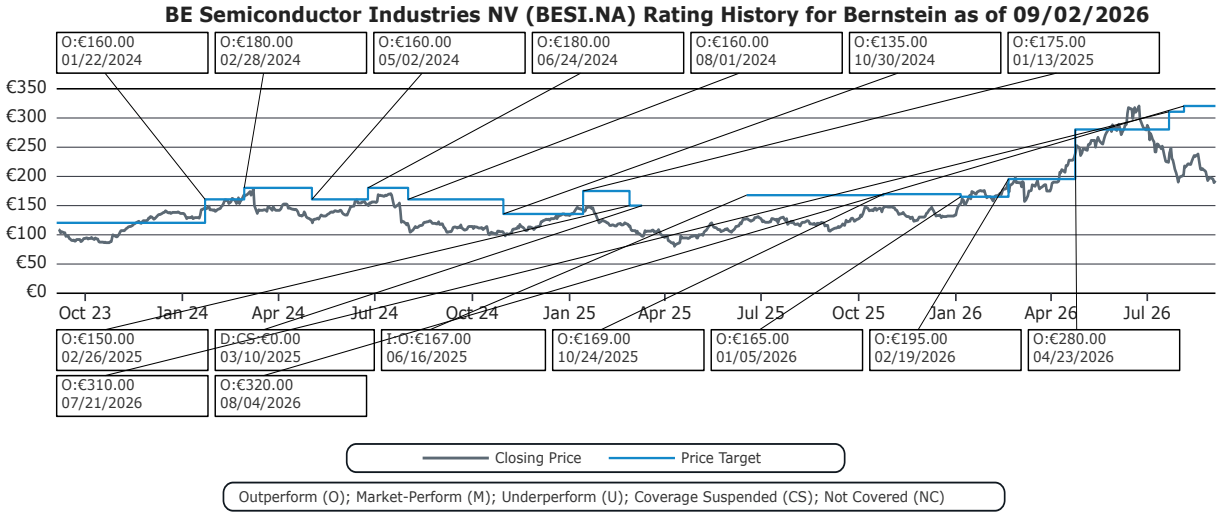
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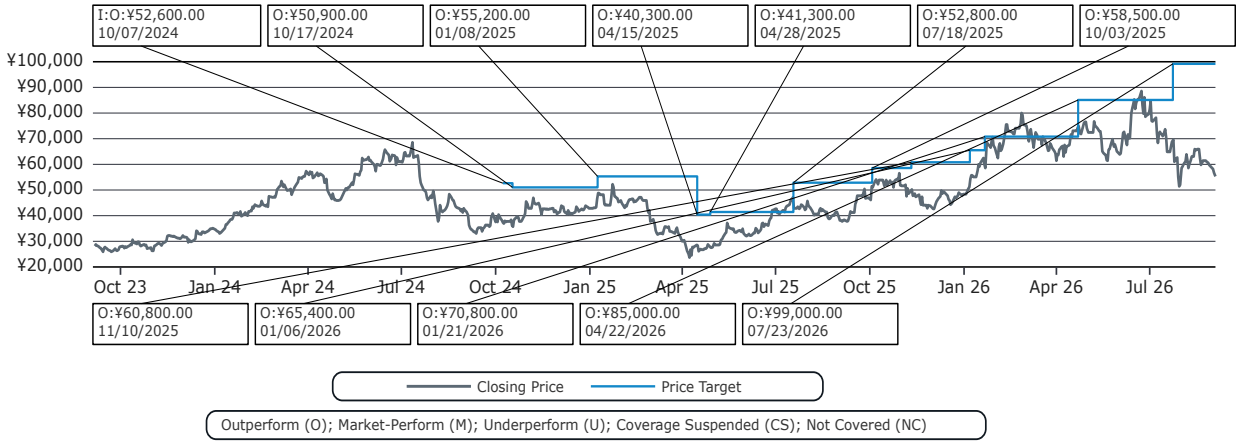
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Outperform	BUY	51.2%	15.3%
Market-Perform (Bernstein Brand) Neutral (Autonomous Brand)	HOLD	35.8%	16.2%
Underperform	SELL	13.1%	13.6%

* These figures represent the percentage of companies within each equity rating category for which affiliates of Bernstein have provided investment banking services within the previous 12 months.
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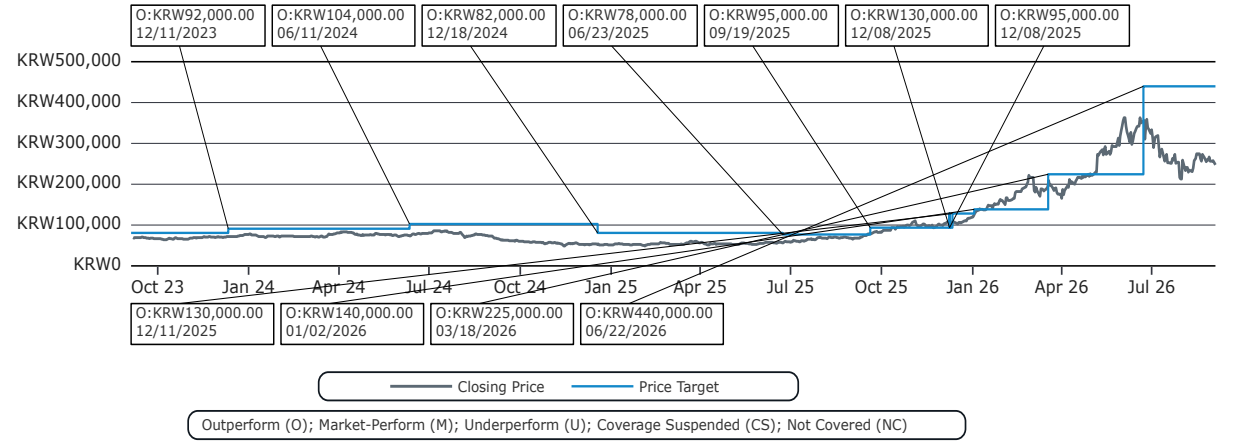
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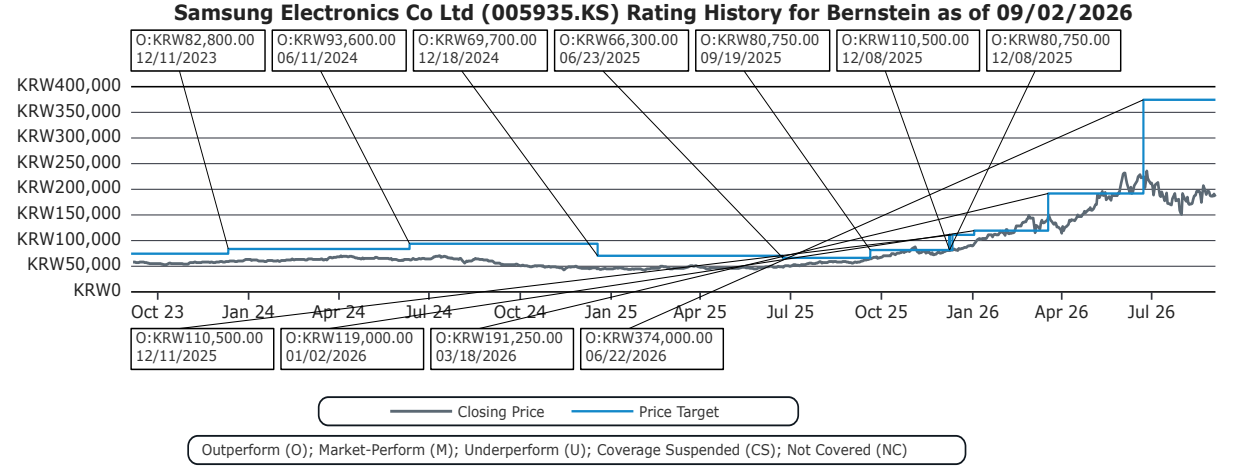
Disco Corp (6146.JP) Rating History for Bernstein as of 09/02/2026



Samsung Electronics Co Ltd (005930.KS) Rating History for Bernstein as of 09/02/2026

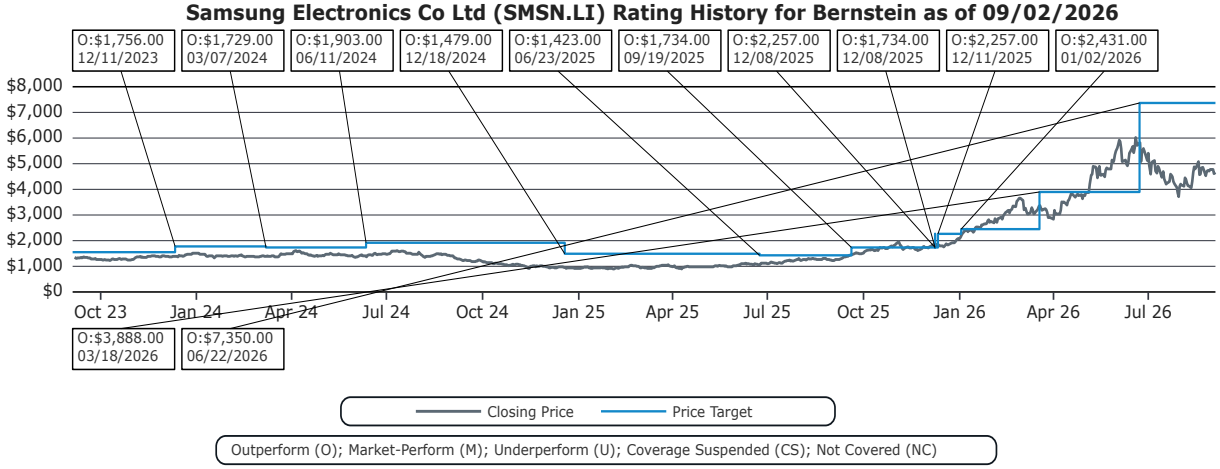


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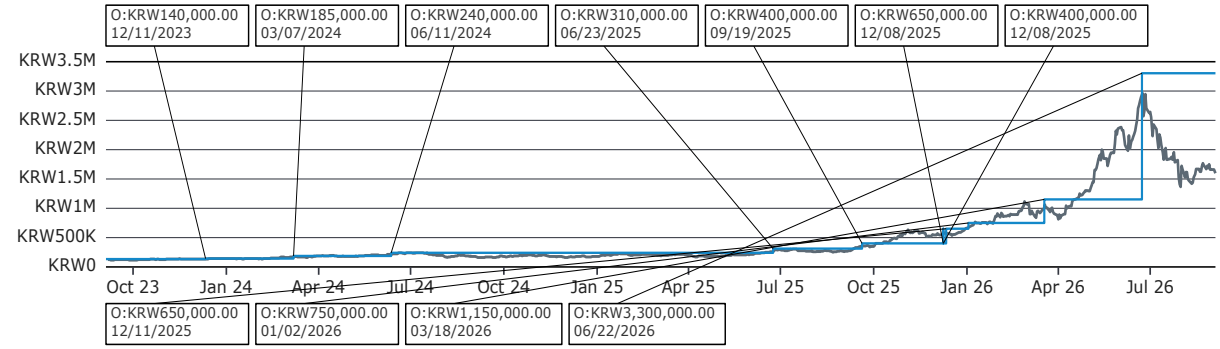
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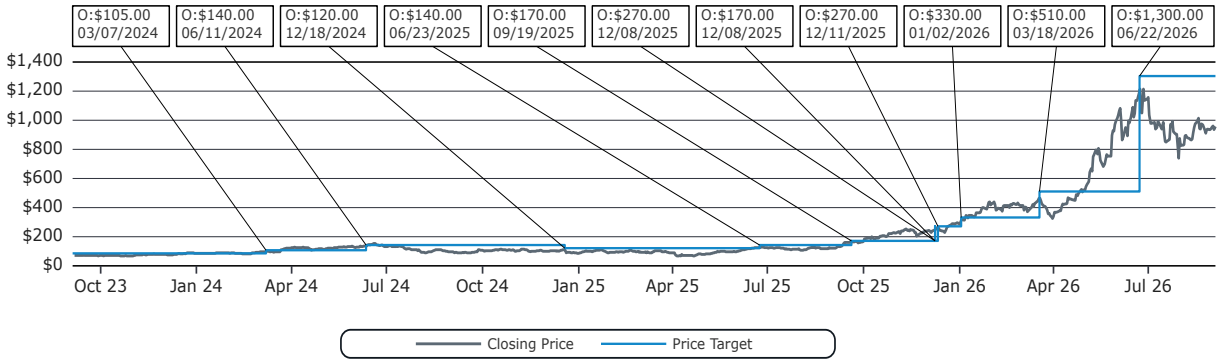
Outperform (O); Market-Perform (M); Underperform (U); Coverage Suspended (CS); Not Covered (NC)

SK Hynix Inc (000660.KS) Rating History for Bernstein as of 09/02/2026

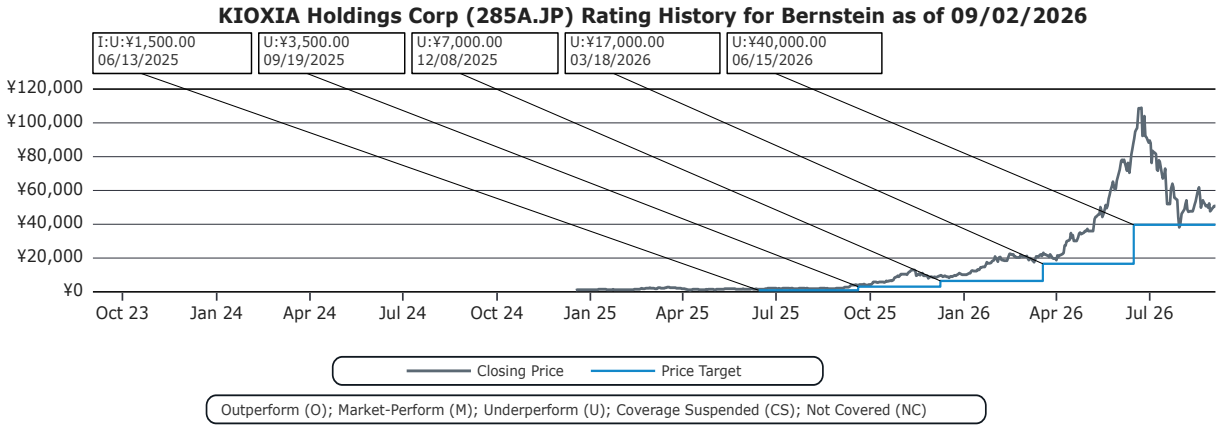


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