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Taiwan Semiconductors

What's New from Citi SEMICON Taiwan Tour – Addressing Advanced Packaging and CPO Manufacturing Opportunities

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We attended SEMICON Taiwan 2026 and hosted investor tours and conferences. Starting from TSMC's presentation, it is pushing CoWoS toward larger package sizes, while SoIC hybrid bonding enables increasingly dense 3D compute and SRAM stacking, making packaging a critical driver of performance, bandwidth, and power efficiency. CPO is the next extension of this architecture, requiring micron-to-sub-micron fiber/FAU coupling, active optical alignment, precision handling, and electro-optical testing. High-volume manufacturing demands higher throughput and early detection of defective devices at wafer and optical-engine levels. This creates a new equipment opportunity combining ATE, probing, optical alignment, coupling, and automation. Overall, advanced packaging is evolving from simply connecting chips into 3D system integration, while CPO is evolving from a silicon-photonics technology into a manufacturing challenge—creating new opportunities across hybrid bonding, precision coupling, optical testing, and automation.

From CoWoS to system integration — TSMC is extending its 3DFabric roadmap from CoWoS-based 2.5D integration toward SoIC 3D hybrid bonding, enabling compute-on-compute and potentially compute-on-SRAM architectures. Larger CoWoS packages, finer-pitch hybrid bonding, and heterogeneous chiplets allow substantially more compute and memory to be integrated within one system. Longer term, TSMC's COUPE silicon-photonics platform could bring optical I/O into this packaging ecosystem, making backend manufacturing almost as strategically important as leading-edge wafer fabrication.

CPO manufacturing bottleneck in alignment and testing — During the CPO manufacturing process, combining EICs, PICs, lenses, and fiber/FAUs may create many challenges. Active coupling uses real-time optical-power feedback and multi-axis positioning to optimize insertion loss, while HVM demands much faster alignment, parallelization, and automated bonding. Testing is another complex process as CPO combines **electrical probing, optical coupling, electro-optical characterization, thermal control, and precision handling** across wafer, optical-engine and final-module stages. Early wafer-level screening is particularly valuable because defective PIC/EIC structures must be identified before expensive downstream packaging. We see various equipment providers entering the CPO testing ecosystem in probing, optical alignment, and coupling automation all around the SEMICON exhibition. We believe key competitive metrics will ultimately be alignment accuracy, insertion loss, throughput, yield and cost per optical engine.

AI demand continues to be strong, yet manufacturing and supply take time to catch up — AI demand remains stronger than supply, while value is shifting toward custom silicon, advanced packaging and testing. Across companies, CPO, chiplet integration, die-to-die connectivity, HBM, shift-left testing and alternative CoWoS-like architectures represent the next growth vectors, with supply availability — not end-demand — remaining the primary limitation through 2027–28.

See Appendix A-1 for Analyst Certification, Important Disclosures and Research Analyst Affiliations

