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Global Memory Interface Chip: Competitive dynamics deep dive



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We highlighted in our memory interface chip industry deep dive that all three major sector vendors (Montage, Renesas, Rambus) will benefit from the agentic AI boom, in the report we provide a deep dive to the competitive dynamics with a focus on Rambus (RMBS, not covered). Our industry model can be downloaded here.

Rambus derives revenue from memory interface chips, DRAM-related IP royalties, and computing-chip IP licensing, exposed to three AI-driven growth engines that should support a strong revenue growth through 2030. Each segment is leveraged to a major secular AI theme: memory interface chips benefit from the server CPU Renaissance driven by agentic AI; DRAM royalties are tied to memory tech migration; and computing-chip IP licensing benefits from growing share of AI ASICs. Together, these businesses provide broad exposure to the core infrastructure layers underpinning AI development. We project the memory interface chip market alone to reach nearly USD 20Bn by 2030. ASIC will account for over two-thirds of CoWoS-based XPU shipments in 2027. Both highlight the magnitude of the opportunities available to Rambus.

However, each of Rambus's core businesses faces competitive constraints that are likely to keep growth below Montage. In memory interface chips, we believe its historical litigation-driven relationship with memory manufacturers limits its ability to gain shares from Montage and Renesas. In DRAM royalties, long-duration licensing contracts provide stable cash flow but inherently cap further growth. In IP for computing chips, Rambus competes against both vertically integrated AI ASIC designers with extensive in-house IP portfolios and ecosystem leaders such as Cadence and Synopsys, whose IP offerings are tightly bundled with EDA tools and foundry workflows. Consequently, Rambus is largely positioned to serve AI chip startups rather than first-tier hyperscaler ASIC programs.

A broader technology portfolio combined with slower revenue scaling should translate into a slower operating leverage than Montage. Rambus invests across memory interface chips, memory controllers, interconnect IP, security technologies, and applications in diverse end markets, resulting in annual R&D spending roughly 40-50% higher than Montage, whose tech portfolio is more focused. While this broad portfolio expands Rambus's addressable market, it also requires a significantly larger engineering organization. Because revenue growth is moderated by the fierce competition discussed above, Rambus generates less revenue per dollar of R&D spending than Montage. Consequently, we expect operating leverage to emerge more gradually for Rambus, leading to slower net income growth than Montage.

We expect Rambus to grow slower than Montage in both revenue and earnings as a result. Market has been trading Rambus at a discount vs. Montage, given slower expected revenue and earnings growth. Nevertheless, a business that rides on 65% TAM growth remains an attractive growth asset.

BERNSTEIN TICKER TABLE

			23 Jul 2026		TTM	Reported EPS				Reported P/E (x)	
Ticker	Rating	Cur	Closing Price	Price Target	Rel. Perf.	Cur	2025A	2026E	2027E	2025A	2026E	2027E
6809.HK (Montage)	O	HKD	311.80	520.00	NA	CNY	1.97	3.21	5.68	136.7	84.0	47.4
688008.CH (Montage)	O	CNY	225.50	400.00	142.3%	CNY	1.97	3.21	5.68	114.5	70.3	39.7
ASIAX			1,880.30									

O - Outperform, M - Market-Perform, U - Underperform, NR - Not Rated, CS - Coverage Suspended

Source: Bloomberg, Bernstein estimates and analysis.

INVESTMENT IMPLICATIONS

We rate **Montage Outperform**, with A-Share TP at CNY 400 and H-Share TP at HKD 520.

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DETAILS

COMPANY OVERVIEW

COMPANY INTRODUCTION

Rambus is a Silicon Valley veteran that has reinvented itself twice - from a memory technology inventor into a patent-licensing house, and over the past decade into a fabless as memory interface chip supplier. Founded in 1990 by Stanford engineers Mike Farmwald and Mark Horowitz and listed on Nasdaq in 1997, the company first rose to prominence with RDRAM, a proprietary high-speed memory interface adopted by Intel around the Pentium 4 era. When the industry standardized on DDR SDRAM instead, Rambus spent the following decade monetizing its patent estate through litigation and licensing against the major DRAM manufacturers, a history we detail in the Royalties business section below. The pivot back to silicon began in 2016 with the acquisition of Inphi's memory interconnect business, which brought DDR4 buffer chips, and accelerated under current CEO Luc Seraphin, who was appointed in 2018 and refocused on memory interface chips.

Today, Rambus operates three revenue pillars: memory interface chips, where it ranks third globally with ~21% share of the core market in 2024; patent royalties from DRAM manufacturers; and silicon IP licensed to computing chip designers. The company generated USD 708Mn of revenue in 2025, up 27% YoY.

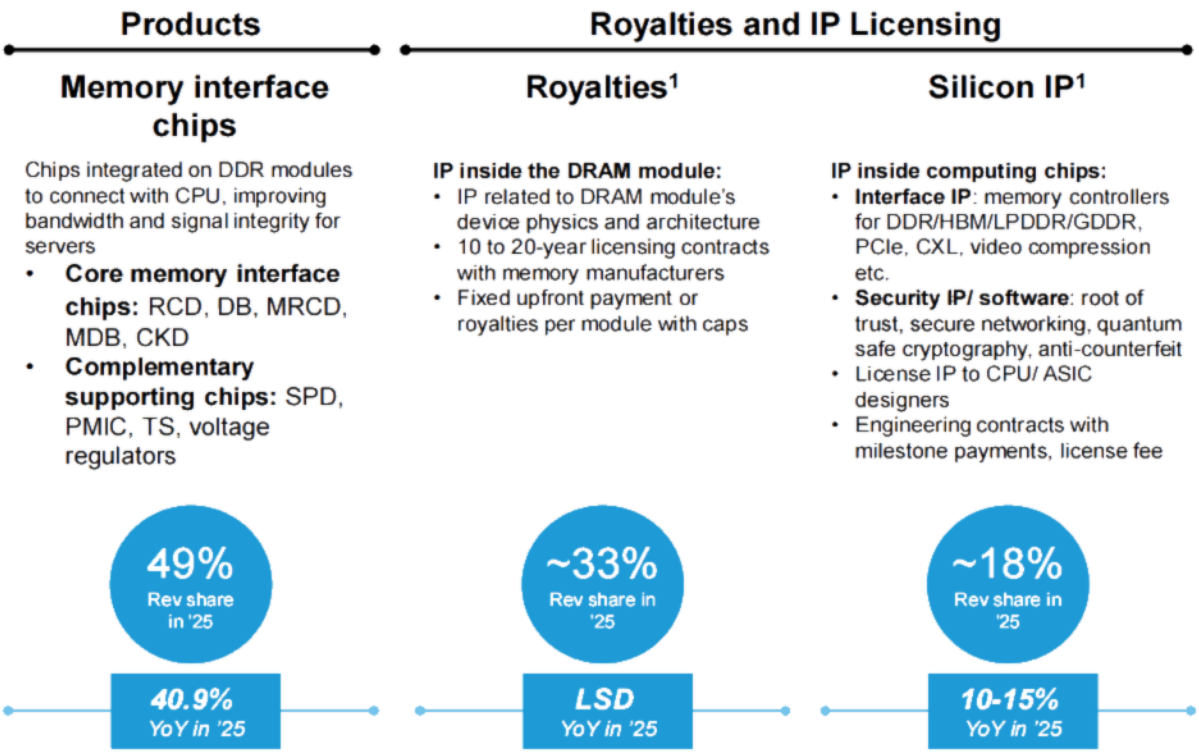
PRODUCT OFFERINGS

Rambus runs two broad business segments, Products and Royalties/ IP Licensing, which are reported in three lines in its financial statements: Product revenue, Royalty revenue, and Contract & other revenue.

The Product line consists of memory interface chips integrated in DDR modules to connect with server CPU, improving bandwidth and signal integrity for servers. This spans the core memory interface chips (RCD, DB, MRCD, MDB, and CKD) and the complementary supporting chips (SPD Hub, PMIC, temperature sensors, and voltage regulators). Product revenue contributed 49% of total revenue in 2025 and grew 40.9% YoY, making it the comany's largest and fastest-growing line.

The Royalties/ IP Licensing segment monetizes two distinct groups of IP for two distinct customer bases, memory manufacturers and computing chip designers. IP inside the DRAM module contributed ~33% of 2025 revenue and grew in LSD YoY. These patents are mainly related to the module's device physics and architecture, licensed to memory manufacturers under 10-20 year contracts structured as fixed upfront payments or per-module royalties with caps. Silicon IP contributed the remaining ~18% of 2025 revenue and is guided to grow at 10-15% YoY. Silicon IP licenses IP inside computing chips to ASIC/ SoC designers, including memory controllers IP for DDR/ HBM/ LPDDR/ GDDR and interconnect IP for PCIe/ CXL, as well as security IP spanning root of trust, secure networking, quantum-safe cryptography, and anti-counterfeit. These engagements combine license fees with engineering contracts carrying milestone payments.

EXHIBIT 1: **Rambus has two primary business segments but reports financial statements in three lines. Two business segments ride on the wave of CPU Renaissance and AI ASIC respectively**



The revenue mix and growth rate numbers are operational approximations per management commentary, not formal reporting segments
Source: company reports, Bernstein analysis

BUSINESS MODEL

The two segments run on fundamentally different business models - one sells chips, the other licenses IP rights.

The memory interface chip Product business is a classic fabless model: Rambus designs the chipsets, outsources fabrication to foundry partners, and sells physical chips to Samsung, SK hynix, and Micron. Revenue scales directly with module volumes and content per chipset, giving the business full exposure to the server memory upgrade cycle.

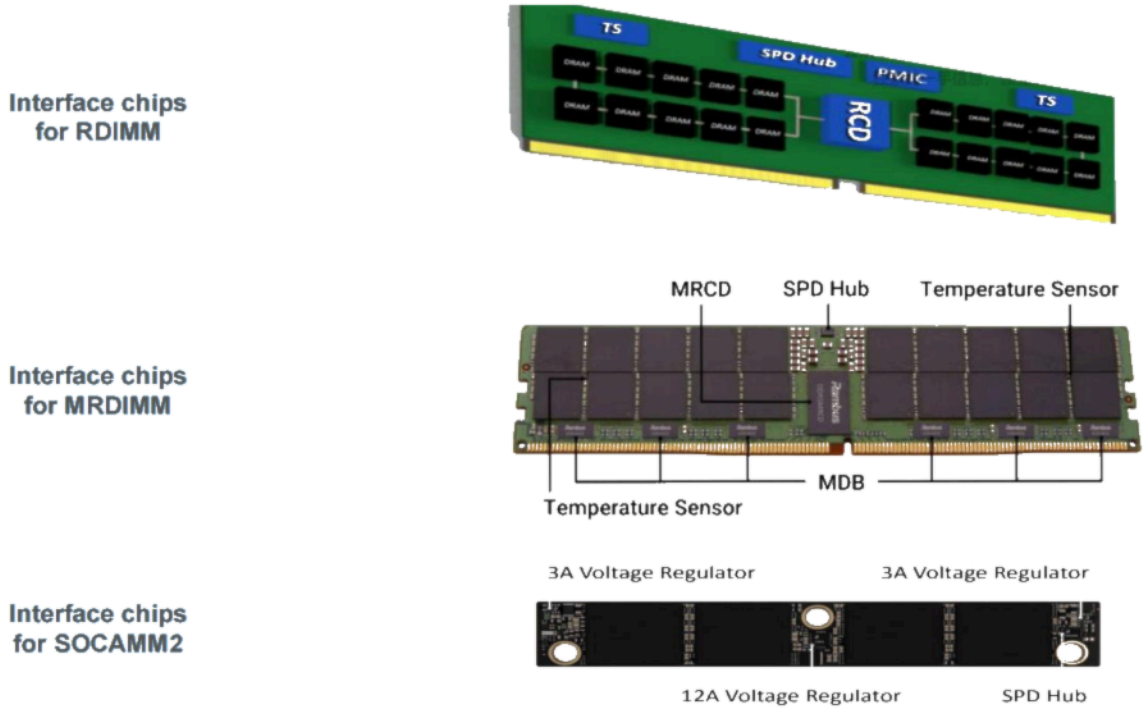
The Royalties and Silicon IP businesses are licensing models: Rambus monetizes intangible assets through long-duration patent contracts and design-win-based IP licenses with engineering milestones. Licensing revenue is extremely high-margin and recurring, but its growth is bounded by contract structures.

Overall, the Product business carries the growth story, while licensing provides the stable cash flow that funds R&D.

MEMORY INTERFACE CHIPS: ACCELERATING TAM GROWTH

As we have elaborated in our memory interface chip primer, **these chips are a core beneficiary of the Agentic AI era, and Rambus enjoys the full strength of this industry beta.** Agentic AI is structurally reshaping demand for server CPUs, DDR memory, and the interface chips connecting them. As workloads shift from GPU-centric training toward inference-heavy agentic deployments, the CPU reclaims its role as orchestrator of multistep, sequential tasks.

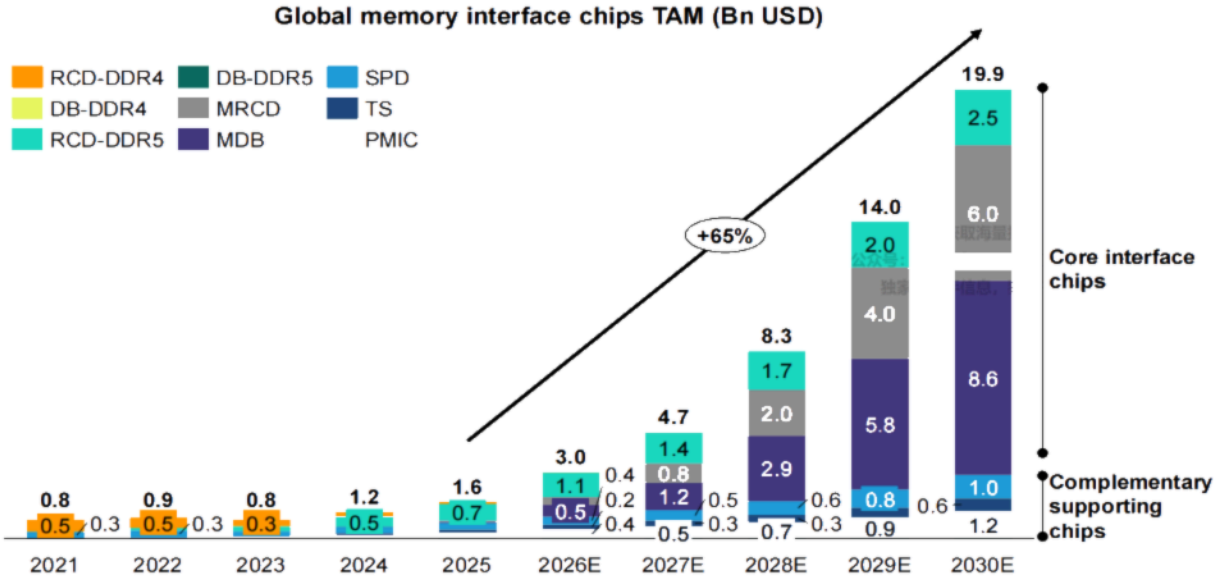
EXHIBIT 2: **Providing memory interface chips for RDIMM & MRDIMM alongside Montage, Rambus is the only supplier of SOCAMM2 interface chips today**



Source: company reports, Bernstein analysis

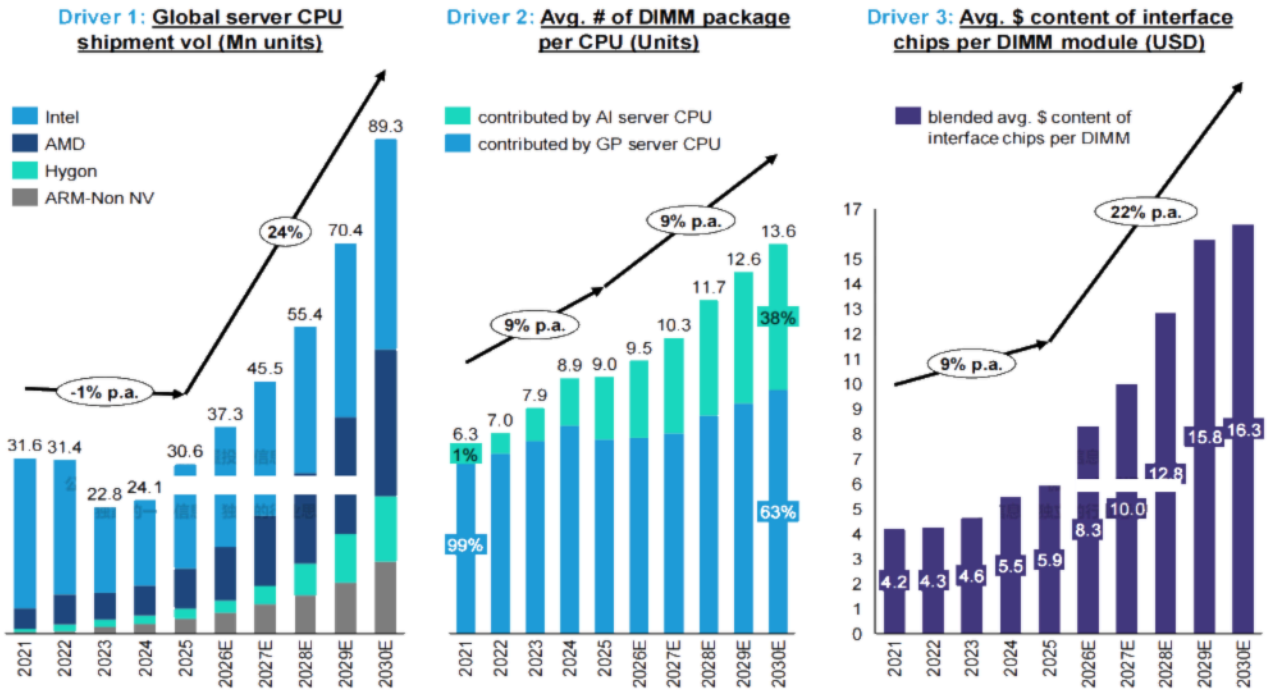
We project the global memory interface chip TAM to grow at ~65% CAGR'25-'30 to reach USD 20Bn in 2030. The strong momentum will be driven by three compounding tailwinds: rising server CPU volumes, more DRAM package per CPU, and higher chipset value per module through the MRDIMM upgrade. MRDIMM is the single largest contributor: we project MRCD and MDB to account for 73% of 2030 TAM, as interface silicon content per MRDIMM module runs roughly 10x that of RDIMM. Importantly, the downside is well protected: even in a bear-case scenario on CPU shipments and MRDIMM penetration, the 2030 TAM still reaches our prior-version projection in $ 8Bn.

EXHIBIT 3: **We raise our global memory interface TAM projection to USD 20Bn in 2030, with MRDIMM's MRCD and MDB contributing 73%, driven by significantly higher chipset value per module**



Our TAM forecast does not include memory interface chips used in NVIDIA proprietary CPUs, such as voltage regulators and PMICs. We expect the impact to be only LSD, as NVIDIA CPUs account for a small portion of server CPU shipments and the related components are of relatively low value.
Source: Mercury, TrendForce, Gartner, Bernstein analysis and estimates

EXHIBIT 4: **The expansion of the TAM is driven by three core factors, each of which is expected to accelerate in the second half of this decade relative to the past 5 years**



Source: Gartner, Mercury, Bernstein analysis and estimates

EXHIBIT 5: **2030 TAM Sensitivity Analysis: Even in a bear-case scenario, the global memory interface chip TAM reaches our prior-version projection, reinforcing a well-protected downside for all memory interface chip suppliers**

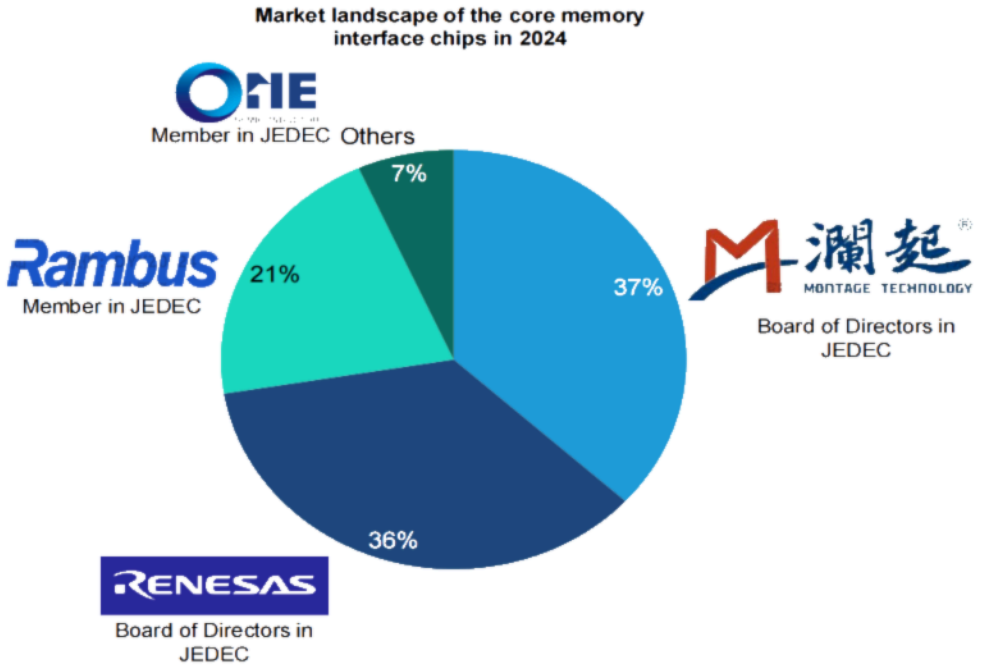
2030 TAM sensitivity analysis (Bn USD)		*Server CPU shipment in 2030 (excl. NV, Mn units)*						
		60	70	80	89	100	110	120
MRDIMM penetration in 2030	10%	8	9	10	12	13	14	16
	15%	10	11	13	14	16	18	19
	20%	12	13	15	17	19	21	23
	25%	13	16	18	20	22	24	27
	30%	15	18	20	23	25	28	30
	35%	17	20	23	25	28	31	34
	40%	19	22	25	28	32	35	38

Source: Bernstein analysis and estimates

Within this expanding market, Rambus competes from the third position in a textbook oligopoly and holds a differentiated footprint across module form factors. The top three players consolidated 90% of the core memory interface chip market in 2024, with Rambus as ~21% behind Montage and Renesas. For DDR5 RDIMM RCD, Rambus management claims that the company is expanding its market share continuously. The company has also closed its historical gap in complementary supporting chips through sequential in-house development since 2022 to pursue a "full chipset" strategy, as management noted that customers increasingly want the whole chipset from one supplier for interoperability reasons at high speed. Now Rambus offers a fully in-house chipset for both RDIMM and MRDIMM, and the management has guided the complementary supporting chips to contribute mid-double-digit percentage of revenue by year end 2026. Notably, Rambus is today the only supplier of SOCAMM2 interface chips, giving it a first-mover position in emerging socket.

As a late entrant to MRDIMM, Rambus has material room to expand share in the segment where the TAM growth is concentrated. Skipping the MRDIMM Gen 1, Rambus directly resources to Gen 2. Starting from a currently almost negligible share base, every Gen 2 design win is incremental: we model Rambus's MRDIMM interface chipset share rising from 2% in 2026 to 18% by 2030, conservatively assuming its long-term market share in MRDIMM chipset lower than that in RDIMM chipset. Meanwhile, management has also guided for continued share gains in complementary supporting chips, where its portfolio build-out is now complete. In short, the company's share trajectory in the highest-growth product category points upward from a low base, a favorable setup relative to competitors defending high shares.

EXHIBIT 6: **The core memory interface chips market is a textbook oligopoly, with top 3 players consolidating 90+% of market share. Rambus is ranked in the 3rd place.**



Source: company reports, Bernstein analysis and estimates

EXHIBIT 7: **Three industry leaders remain closely matched in DDR5 RDIMM and MRDIMM offerings. However, Rambus is the late entrant in MRDIMM memory interface chips**

		Mass production		Sampling	R&D
Product roadmap of chipsets for DDR5 RDIMM	澜起	DDR5 Gen 1 4800MT/s	DDR5 Gen 2 5600MT/s	DDR5 Gen 3 6400MT/s	DDR5 Gen 4 7200MT/s In Oct '25	DDR5 Gen 5 8000MT/s In 4Q24	DDR5 Gen 6 9200 MT/s In 2Q26
	RENESAS	DDR5 Gen 1 4800MT/s	DDR5 Gen 2 5600MT/s	DDR5 Gen 3 6400MT/s	DDR5 Gen 4 7200MT/s	DDR5 Gen 5 8800MT/s	DDR5 Gen 6 9600MT/s In Nov '25
	Rambus	DDR5 Gen 1 4800MT/s	DDR5 Gen 2 5600MT/s	DDR5 Gen 3 6400MT/s	DDR5 Gen 4 7200MT/s	DDR5 Gen 5 8000MT/s In Oct '24	DDR5 Gen 6
Product roadmap of chipsets for DDR5 MRDIMM	澜起	MRDIMM Gen 1 8800MT/s Product introduction and sampling in 2022			MRDIMM Gen 2 12800MT/s Sampling in Jan '25, backlog to be delivered in 1H26 worth 20Mn USD		
	RENESAS	MRDIMM Gen 1 8800MT/s Product introduction and sampling in 2022			MRDIMM Gen 2 Sampling in Nov '24		
	Rambus				MRDIMM Gen 2 12800MT/s Sampling in Oct '24		

Source: companies official websites, Bernstein analysis

However, we believe Rambus's market share is structurally capped, owing to its historical delicate rela memory manufacturers. Rambus's history is deeply rooted in patent enforcement and litigation against the DR

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who are the customers and co-validation partners that memory interface chip vendors depend on. While this strategy built a valuable intellectual property portfolio, we believe the legacy relationship may constrain Rambus's ability to achieve a dominant position. DRAM makers control module qualification and favor suppliers with whom they have deep co-development trust, the dual-sourcing preferences naturally distribute share toward the two competitors. We expect Rambus to continue gaining share as MRDIMM adoption accelerates, but we believe its long-term share in MRDIMM interface chips is likely to be restricted to the third position, given the competitive landscape and customer dynamics.

ROYALTIES OF IP INSIDE THE DRAM MODULE: STABLE BUT LOW-GROWTH

Two decades of patent litigation converted Rambus's IP estate into a recurring royalty annuity, the origin of today's second-largest revenue line. The campaign began with the Infineon suit in Aug 2000, the first major test of Rambus's DDR patent claims, and ran through the FTC's antitrust action over Rambus's conduct at the JEDEC standards body, removing the principal legal overhand and preserving the enforceability of the patent estate. A jury verdict in Rambus's favor against SK hynix and Micron in 2008 then set the stage for negotiated settlements with all three major DRAM makers: Samsung in 2010, and SK hynix & Micron in 2013. These settlements have since been renewed and extended into the 10-20 year licensing contracts that underpin the segment today.

EXHIBIT 8: **Two decades of patent litigation converted Rambus's IP estate into recurring royalties revenue. But we think this delicate relationship with memory vendors may structurally restrict its share in interface chip sector**

Counterparty / Case	Period	Forum	Core issue	Outcome	Legacy for Rambus today
Infineon Technologies	Aug 2000 - 2005	U.S. federal courts (E.D. Va.; Fed. Cir.)	Alleged infringement of Rambus patents by DDR SDRAM; Infineon counterclaimed fraud over JEDEC conduct	Settled in 2005 with a patent license agreement (terms per press reports)	First major litigation converted to license; template for later settlements
U.S. FTC, Docket 9302	2002 - 2008	Federal Trade Commission; D.C. Circuit	Antitrust: alleged deception of the JEDEC standards body while patenting standard-essential technology	FTC ruled against Rambus (2006); decision overturned on appeal (2008)	Removed the antitrust overhang; preserved enforceability of the patent estate
Hynix / Micron (coordinated trials)	2000s - Mar 2008	U.S. federal courts (N.D. Cal. and others)	Patent infringement and JEDEC-conduct defenses tried across coordinated proceedings	Jury verdict rendered March 26, 2008 in Rambus's favor on key issues	Set the stage for negotiated settlements with all three major DRAM makers
Samsung Electronics	Settled Jan 2010	Settlement agreement	Resolution of all outstanding patent claims	Agreement valued at ~$900Mn, including a $200Mn upfront payment and a $200Mn purchase of Rambus stock (per contemporaneous press reports)	Largest single settlement; anchor licensee relationship, since renewed
Rambus v. Nvidia	2008 - 2010	U.S. ITC and federal courts	Alleged infringement of Rambus memory controller patents	Nvidia entered a patent license agreement with Rambus (2010, per press reports)	Extended licensing beyond DRAM makers to logic/GPU designers
SK hynix	Settled Jun 2013	Settlement / license renewal	Resolution of the long-running Hynix patent dispute	$240Mn five-year license, structured as $12Mn per quarter	Recurring royalty stream, since extended into a long-term agreement
Micron Technology	Settled Dec 2013	Settlement agreement	Resolution of the final major DRAM patent dispute (RDRAM/DDR era)	Seven-year agreement worth up to $280Mn	Completed licensing coverage of all three major DRAM manufacturers

Source: SEC filings, Bernstein analysis

The result is a stable, annuity-like revenue stream, but one that management has guided to remain largely flat, offering limited growth. The agreements are structured as fixed upfront payments or per-module royalties with caps, which insulates the stream from DRAM cycle volatility but equally excludes Rambus from expanding in the current DRAM volume and pricing upcycle. We view this segment as a dependable cash generator that funds the company's R&D, but not a source of growth, a distinction that matters for the company-level growth profile discussed in the following sections.

LICENSING IP INSIDE THE COMPUTING CHIPS: ATTRACTIVE END MARKET, BUT INTENSE COMPETITION

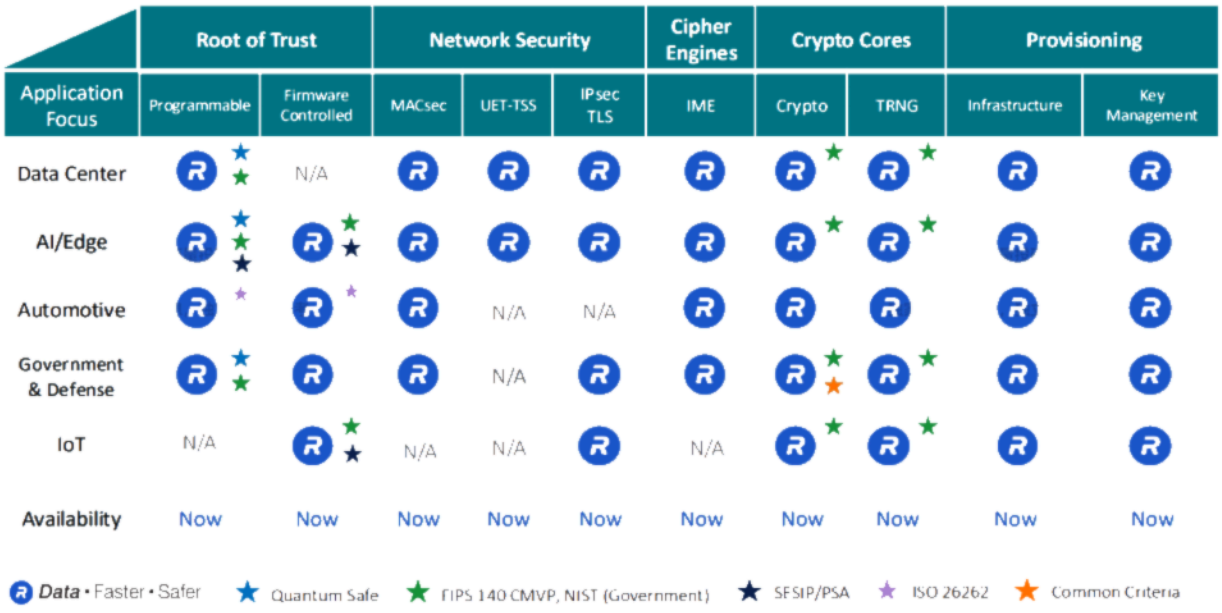
The addressable market for memory controllers and interconnect IP used in computing chips is expanding rapidly, driven by the strong demand for custom AI ASICs. Our global semi team projects AI ASIC can reach 20% of the XPU market by value in 2027, up from 10% in 2026. Measured by shipment volume, Bernstein projects ASIC will account for over two-thirds of CoWoS-based XPU shipments in 2027. ASIC benefits from the industry's inflection from training to inference and will grow faster than the broader accelerator market. CSP, including Google, Microsoft, Amazon, and Meta, are accelerating ASIC adoption to improve performance per dollar, lower total cost of ownership, and reduce reliance on external GPU supply chains. Every one of these custom ASIC chips needs HBM and DDR controllers, interconnect, and security IP, which are exact portfolio Rambus licenses.

EXHIBIT 9: **A diversified IP business spanning memory controllers, interconnect controllers, and security tech drives higher R&D intensity than Montage (1/2)**

	Memory Controllers						Interconnect Controllers					Video Compression	
	DDR	LPDDR	GDDR	HBM			CXL		PCI Express		MIPI	VESA	FEC
Application Focus	4	4X/5X/5T	6/7	2/2E	3/3E	4/4E	2.0	3.1	6.3	7.0	CSI-2/ DSI-2	DSC/ VDC-M	DP/ HDMI
Data Center		®	®	®	®	®	®	®	®	®			
AI/Edge		®	®	®	®	®	®	®	®	®			
Automotive	®	®	®						®		®★	®★	®★
Government & Defense	®								®				
IoT		®									®	®	®
Availability	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now

Source: company reports

EXHIBIT 10: **A diversified IP business spanning memory controllers, interconnect controllers, and security tech drives higher R&D intensity than Montage (2/2)**



Source: company reports

However, we think Rambus faces intense competition in this attractive market, from two structurally advantaged groups.

- **Leading AI ASIC design parters, such as Broadcom, Marvell, and MediaTek, possess extensive in-house expertise and proprietary portfolios of memory controllers and interconnect IP, leaving little room for third-party licensing within their hyperscaler programs**. These capabilities are the by-product of decades of shipping connectivity-intensive silicon at scale, hardened across thousands of tape-outs rather than developed for licensing. Broadcom refined its industry-leading SerDes and HBM PHY/ controller stack through successive generations of networking switch silicon and custom accelerator engagements, especially Google TPU program it has served across multiple generations. Marvell built its portfolio on storage and networking controller heritage and reinforced it through acquisition - Avera (the former IBM/ GlobalFoundries ASIC design unit) in 2019 and Inphi's high-speed interconnect franchise in 2021. MediaTek's high-volume smartphone SoC business has kept its DDR memory controllers silicon-proven at leading-edge nodes for over a decade. Qualcomm has internal heritage developed through smartphone SoC, but also acquired Alphawave in 2025, which provides high-speed connectivity IP to AI datacenter. Because memory controller and interconnect IP portfolios are the performance-critical portion of an AI ASIC, these vendors treat it as core differentiation for winning whole-chip engagements, resulting in bundling the IP within the design contract rather than sourcing it externally.

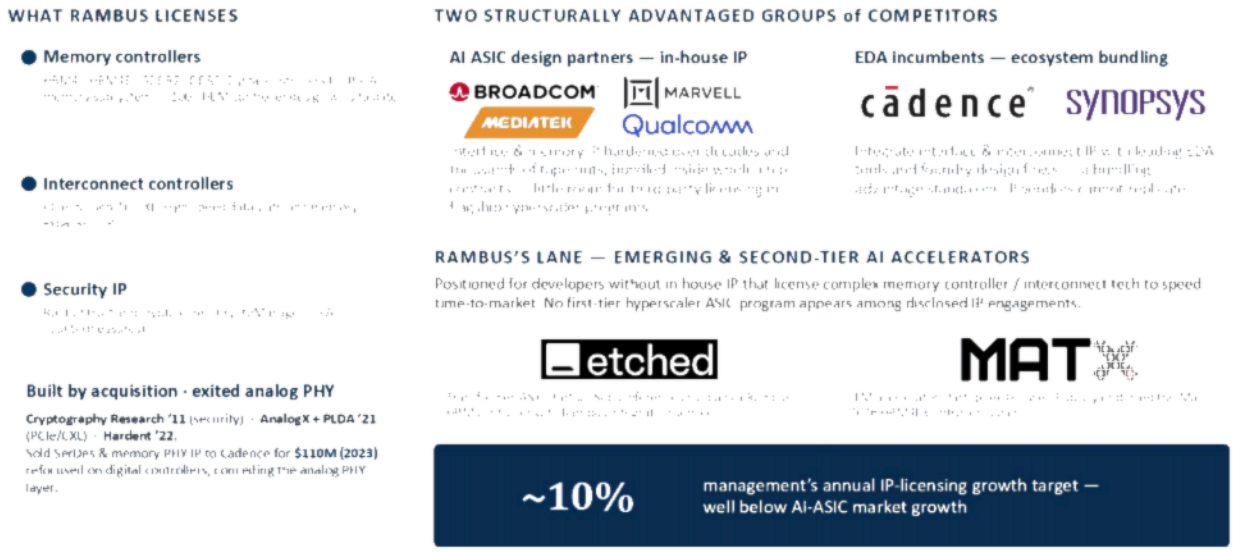
- **Cadence and Synopsys benefit from strong ecosystem advantages, integrating their controllers, PHY, and interconnect IP offerings with industry-leading EDA tools and foundry design flows**, a bundling that standalone IP vendors cannot replicate. Rambus has already conceded ground where this bundling bites hardest, because it sold its SerDes and memory PHY IP business to Cadence for USD 110Mn in 2023 and exited the analog PHY layer to refocus on digital controller IP.

Given these dynamics, Rambus is primarily positioned to serve emerging or second-tier AI accelerator developers that lack internally developed IP and prefer to license complex memory controllers and interconnect technologies to accelerate product development. The customers Rambus showcases are precisely the emerging AI silicon designers we would expect: Etched, the transformer ASIC startup whose Sohu inference chip pairs a Rambus HBM memory controller with Rambus integration services to complete the memory subsystem; and MatX, the LLM accelerator startup founded by former Google engineers, which publicly endorsed the Mar 2026 HBM4E controller launch. Notably, no GPU or first-tier hyperscaler ASIC program appears among its disclosed IP engagements, with those sockets being locked up by the ASIC design partners' in-house IP. We believe this competitive backdrop explains why management is targeting only approximately 10% annual growth for the IP Licensing to

computing chips business, despite the rapid expansion of the broader AI ASIC industry.

Looking further ahead, we believe a more meaningful growth opportunity could emerge in edge AI over the mid to long term. Unlike the hyperscaler AI accelerator market, where a handful of CSPs concentrate design activities with selective leading ASIC partners, edge AI chip development is likely to be far more fragmented, spanning automotive, IoT, and industrial applications. A long tail of chip designers with limited in-house expertise creates structurally greater demand for outsourced memory controller and interconnect IP solutions, and Rambus's breadth across memory, interconnect, and security IP positions it well to capture this demand as the market matures.

EXHIBIT 11: **Rambus has to compete with two groups of advantaged competitors in IP licensing for computing chips business, resulting in much slower segment growth expectation than the rapidly-expanding AI ASIC downstream market**



Source: company reports, Bernstein analysis

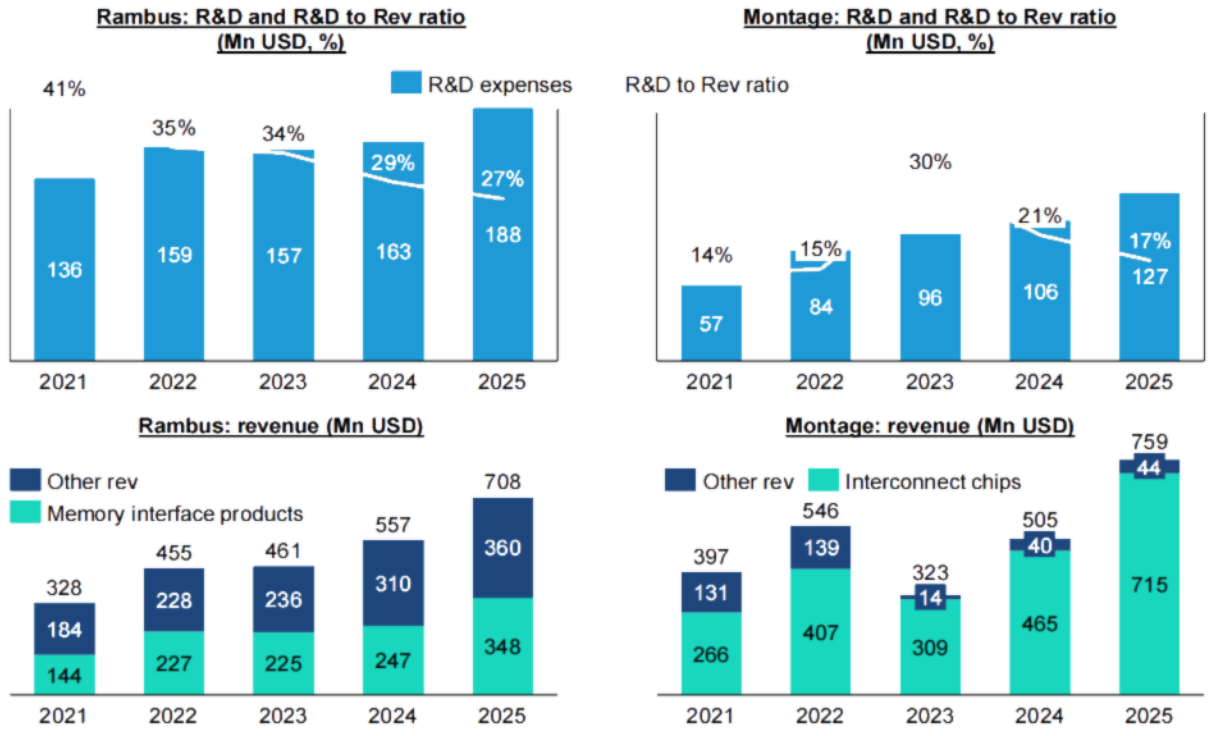
Nevertheless, royalties and IP licensing businesses in lower growth rate dilute the company's overall growth profile. The relatively low-growth licensing and contract businesses, two segments guided flat and ~10% annual growth respectively, still represent roughly half of total company revenue in 2025. As a result, we expect company-wide revenue growth to trail that of Montage, whose lower-growth businesses account for only an LSD percentage of total revenue.

MODERATE OPERATING LEVERAGE AND EARNINGS GROWTH RESTRICTED BY R&D INTENSITY

Rambus maintains a significantly broader technology portfolio than Montage, which results in annual R&D spending approximately 40-50% higher. Apart from the overlapping memory interface chips portfolio, the IP business alone spans memory controllers across DDR/LPDDR/GDDR/HBM, interconnect controllers across CXL and PCIe, video compression, and a full security stack from root of trust to quantum-safe cryptography. Each of these tech IP demands sustained R&D and engineering spending across data center, automotive, government, and IoT end markets. Rambus spent USD 188Mn for R&D in 2025, versus USD 127Mn for Montage.

Meanwhile, Rambus generates lower revenue relative to its larger R&D investment, leading to a substantially higher R&D-to-revenue ratio than Montage. We believe the lower revenue results from its lower market share in the key memory interface chip market, partly a consequence of the historical relationships with memory vendors discussed above. Exhibit 12 shows Rambus's R&D-to-revenue ratio stood at 27% in 2025, versus 17% for Montage. Given that R&D expenses account for more than 60% of Rambus's total operating expenses, R&D efficiency is the critical driver of long-term earnings growth. In our view, Rambus is likely to realize operating leverage more gradually than Montage as revenue scales.

EXHIBIT 12: **Rambus's broader tech portfolio and lower market share lead to higher R&D expenses and lower efficiency, compared to more focused Montage**



Source: Bloomberg, Bernstein analysis