

Memory Market Update

Implications from NVDA Computex speech, SEC/SKH new HBM concept disclosure, and Kioxia investor day

Over the last couple of days, multiple industry and company events were held in Asia and we share key implications to the memory industry in this report. Overall impressions remain positively biased, confirming the ongoing memory value share gain trajectory in the AI ecosystem and we maintain our bullish stance on the multi-year up-cycle thesis. Key OW names in Asia are: **SEC**, **SKH**, and **Kioxia**.

- NVDA Computex event's implications for the memory industry.** We believe Mr. Jensen Huang's commentaries were broadly in-line, reconfirming the current industry developments: 1) Vera CPU adding fuel to existing memory demand as Mr. Huang emphasizes Vera CPU as the major incremental growth driver of the company adopting PCIe 6 with LPDDR5X memory at 1.2TB/s (JPMc: 0.6M/3M Vera CPU in 26/27E with SOCAMM TAM also reaching ~30bn/~80bn Gb in 26/27E); 2) confirmation of Vera Rubin rack entering full scale production syncing with HBM4 bit crossover in 2H26E, albeit Rubin shipment is somewhat suppressed by HBM4 supply, in our view ([Asia Tech Computex Takeaway Part 1](#) for details); and 3) new product releases such as the N1X for AI PC adopting 128GB of LPDDR5X (8 modules of 16GB LPDDR5X), materially higher than the average PC content of 12-16 GB. We believe that the Agentic AI workloads continued to be a key focus during the presentation, reinforcing the need for memory to power AI agents and tokens, of which QCOM's CEO is projecting the token consumption to grow 40x from 2026 to 2030E due to the rapid rise of on-device AI and intelligent agents. Faster edge AI device takeoff could be an upside risk to long-term Mobile/PC memory demand estimates.
- SK Group Chairman, Mr. Chey Tae-won, lays out 2x SKH DRAM WSPM increase plan over next five years; peak-out signal or vigorous plans to address shortage?** Historically speaking, memory suppliers' capacity overbuild commentary has been taken negatively by the investor community. In many cases, demand projections were always full of uncertainty and pricing in the risk was a natural reaction from the stock market. We echo the chairman's commentary of a significant shortage through 2030 (JPM base case: shortage worsening in 2027E vs. 2026E and absolute shortage trend continuing into 2028E - [latest JPM GMM S-D view](#) for details) and view the capacity buildout as a sign of a healthy shortage debottlenecking process. SKH held 530k DRAM WSPM as of 2025-end (350k in Korea and 180k in China) and we forecast 745k/865k by 2028-end/29-end. Over a million WSPM implies SKH potentially filling in the entire Yong-in cluster no.1 (comprising of six phases) by the end of 2030E with each phase capacity as high as 70k on top of M15X 80k WSPM. We believe multiple variables need to be addressed, such as EUV equipment readiness (well over 50 tools will be needed from 2028E-2030E, in our view) and EPC infrastructure buildout constraints (SKH's official infrastructure completion target is by December 2030 - [note](#)).
- SEC and SKH unveil next-gen HBM roadmap and technology - all about heat control.** Korean memory makers showcased new heat control concepts;

Technology - Semiconductors

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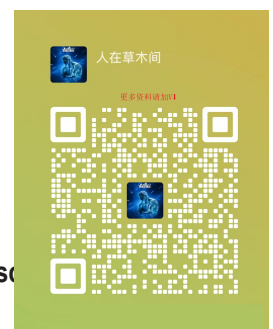
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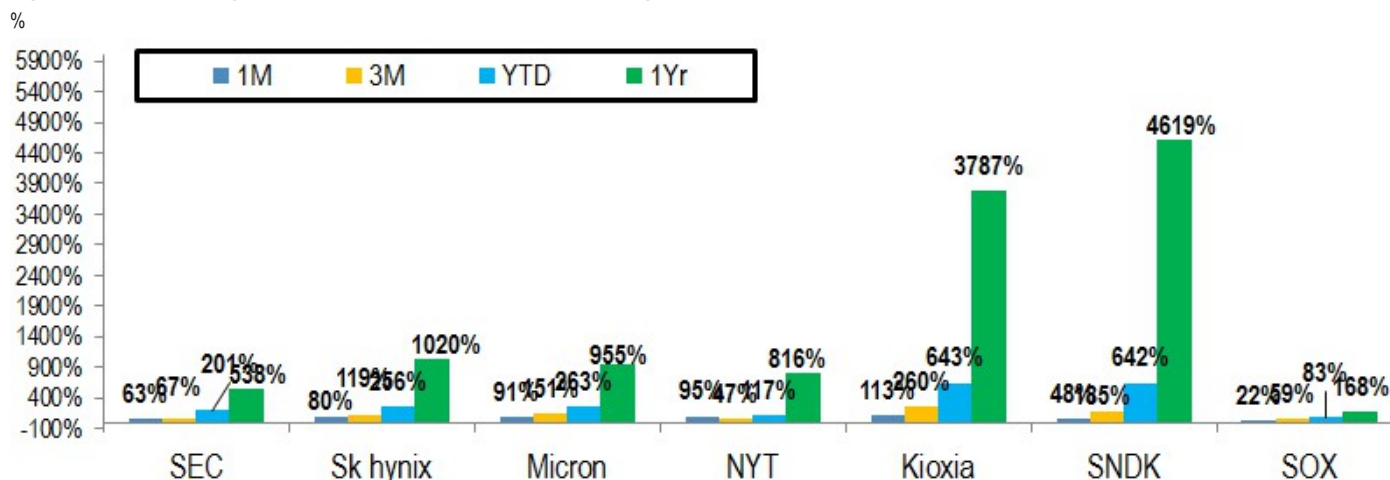
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SEC - HPB (Heat Path Block) and SKH - iHBM (Integrated Cooling Elements, ICE); to be used in next-generation HBM products. SEC's HPB (likely made of silicon due to its superior thermal conductivity) was designed to effectively distribute and dissipate the heat from the die-to-die surface. Investors raised questions if HPB forces DRAM core die design to be shrunk; therefore, die design compatibility with 2nm GAA will be the key monitoring points on HPB design progress, in our view. The company also unveiled its plans to use 2nm GAA for base dies in HBM5 (vs. 4nm base dies in HBM4/4E) and reported a maximum pin speed at 16Gbps (bandwidth: 4TB/s). As for SKH, iHBM concept was heavily discussed and the company reported 30% heat dissipation improvement via incorporating ICE (made of silicon) targeting mass adoption from HBM5 ([link](#)). The iHBM solution places the ICEs directly in the die-to-die physical layer area where heat concentration is the highest, creating an additional heat dissipation path. These approaches are likely to alleviate the ongoing heat dissipation concerns in the HBM amidst growing performance requirements for the entire AI stack system.

- Kioxia Investor Day event takeaways.** We came away with a positive impression from the Kioxia Investor Day event yesterday (*Kioxia company [note](#) for details*), where the company a) revised up long-term NAND TAM estimates to 1,807EB by 2028E (implying +22% CAGR in the next three years vs. formal view of ~20% CAGR) with S-D tightness continuing at least throughout 2027E; b) laid out eSSD segmentation (eSSD TAM to reach above 900EB by 2028E from 295EB in 2025A with fastest growth segment being inference: +86% CAGR outpacing overall eSSD CAGR of +46%) with clear growth strategy leveraging BiCS/CBA technology (different eSSD solutions based on SLC, TLC, and QLC), and c) maintained disciplined capex spending policy utilizing fab space from Yokkaichi Fab 7 (Y7) and Kitakami Fab 2 (K2) before pivoting Kitakami Fab. We also sense smooth progress in LTA discussions between Kioxia and key customers; multi-year LTA traction is extending beyond 2029 and LTA is likely to cover nearly half of the total business. Lastly, on the shareholder return side, the progressive dividend framework (potentially as early as 2H FY26, funded from excess cumulative FCF). While Kioxia team's NAND S&D commentary appears to be consistent with our latest GMM S-D outlook (JPM 2028E NAND TAM at 1,869EB), the JPM memory research team takes a more aggressive view on eSSD TAM CAGR vs. a conservative view on consumer grade NAND.

Figure 1: Global memory makers' share price performance including SOX (Philadelphia Semiconductor index)



Source: Bloomberg Finance L.P.