Semiconductors

AI Drives Resurgence in Custom Chips (ASICs) - ASIC Market Overview/Update

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What Is An ASIC??

ASIC – Application Specific Integrated Circuit:

- **A chip that is designed for a specific CUSTOMER for a specific application or platform:**
  - Example: Apple iPhone A19 processor chip (Apple does complete design)
  - Example: Nokia Reef Shark BTS processor chip (Nokia, Marvell, Broadcom)
  - Example: Google TPU AI processor (Google, Broadcom)
  - Example: Amazon Trainium 3 AI processor (AWS, Marvell, Alchip)

ASSP - Application Specific Standard Product (sometimes called "merchant")

- **A chip that is designed for multiple customers for a specific application:**
  - Example: Qualcomm snap-dragon mobile processor family
  - Example: NVIDIA AI GPU, AMD AI GPU

GP - General Purpose products – multiple customers/multiple applications

- A chip that is designed for multiple customers for multiple applications
  - Example: Intel/AMD PC or server CPU
  - Example: Infineon, STMicro, Onsemi – power semiconductors/Microcontrollers
  - Example: Samsung, Hynix, Micron – memory/storage

Market Sizing (2025)

Total Semi Industry Revenues CY25

$805B

Application Specific

$351B

General Purpose

$454B

Application Specific Standard Products (ASSPs)

$282B

- AI GPUs (NVDA, AMD)
- Qualcomm Snapdragon
- In vehicle SDV Processor
- Networking switch IC
- Optical DSP IC

Application Specific Integrated Circuits (ASICs)

$68B

- Google TPU AI Processor
- Nokia Reef Shark 5G RAN
- Amazon Trainium XPU
- Apple A19 iPhone CPU
- Apple iPhone wireless charging
- Microsoft Maia AI processor

Memory

Microprocessor

Analog

Power

Why Design Your Own ASIC or Custom Chip?

Value proposition of doing your own custom chip or ASIC:

- Customer OWNS the software stack
- If you own the software stack, can custom tune the silicon to the specific software stack and driver better system level performance (compute performance/power)
- The economics (high volume applications and /or high ASP infrastructure platforms lend themselves well to ASICs) – need to drive ROI/Justification of customer silicon chip design team:
- **Apple is the poster child for custom ASICs –** they create/own the entire software stack/applications layer, they own the entire system design, they can differentiate on platform performance/low power and they ship 250M units per year (strong ROI on internal chip design R&D) – leverage investments into PC CPUs, watch CPUs, etc…
- **Game consoles (Sony/Microsoft) –** same value prop as Apple – relative high volumes
- **Base station RAN processor ASICs –** small volumes, but VERY HIGH ASPs, leverage across entire network/subscriber base drives ROI
- **Google TPU AI processor, Amazon Trainium AI processor, Meta MTIA processor, Microsoft Maia AI processor –** low volumes, but VERY VERY HIGH ASPs – token generation/AI monetization will drive strong ROI

Example: AI GPU Versus AI Custom ASIC Processor

AI ASICs/XPUs Offer Competitive Performance, Economics and Power Efficiency

	NVIDIA B200 Blackwell	NVIDIA B300 Blackwell Ultra	Google/ Broadcom TPU7x Ironwood
Compute performance (FP8 TFLOPS)	4500	5000	4614
Memory capacity per chip (HBM3E)	192	288	192
HBM bandwidth per chip (TBps)	7.7	8.0	7.4
TDP (Watts)	1000	1200	1000
ASP	$35,000	$40,000	$13,000
TFLOPS per $	0.13	0.13	**0.35**
TFLOPS per Wattt	4.50	4.17	**4.61**

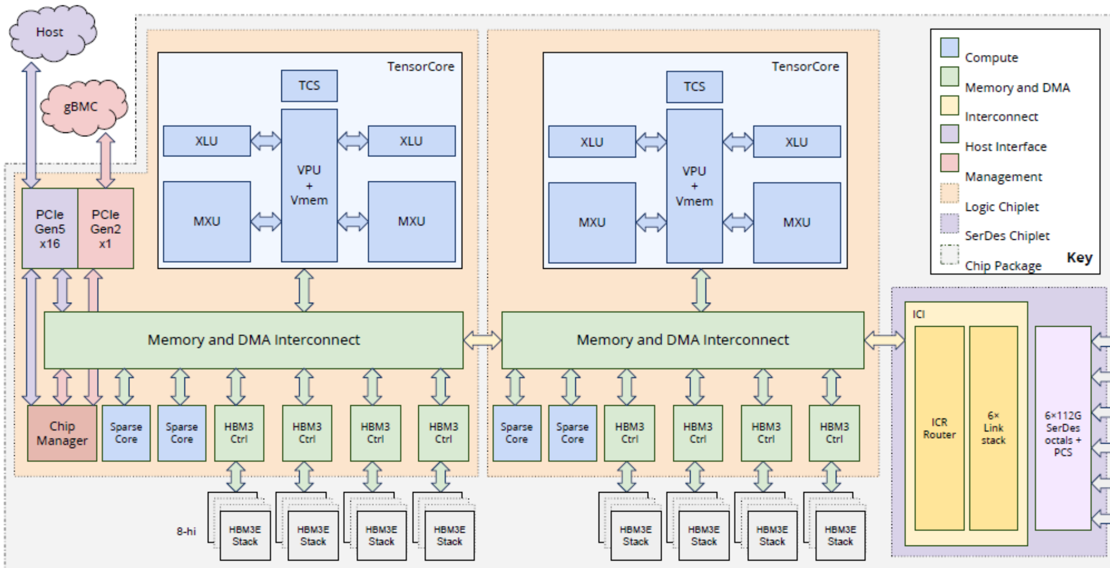
Compute Platform Partner	Scenario	DC Capex per GW	Compute Partner Revenue per GW	Compute Capex	Networking Capex
NVIDIA	*Low case*	$45	$20	$16	$4
	High case	$55	$30	$24	$6
AMD	*Low case*	$35	$15	$14	$2
	High case	$40	$20	$18	$2
Broadcom	*Low case*	$30	$10	$7	$3
	High case	$40	$15	$11	$5

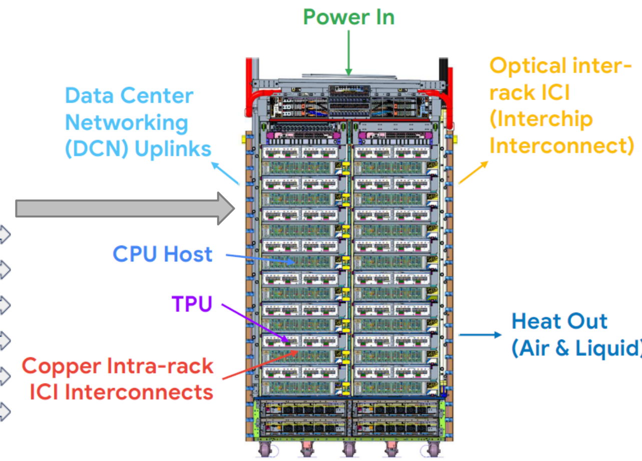
Source: Company reports, J.P. Morgan research

Chip and Rack Architectures – TPU7x Ironwood ASIC vs. Nvidia Blackwell GPU

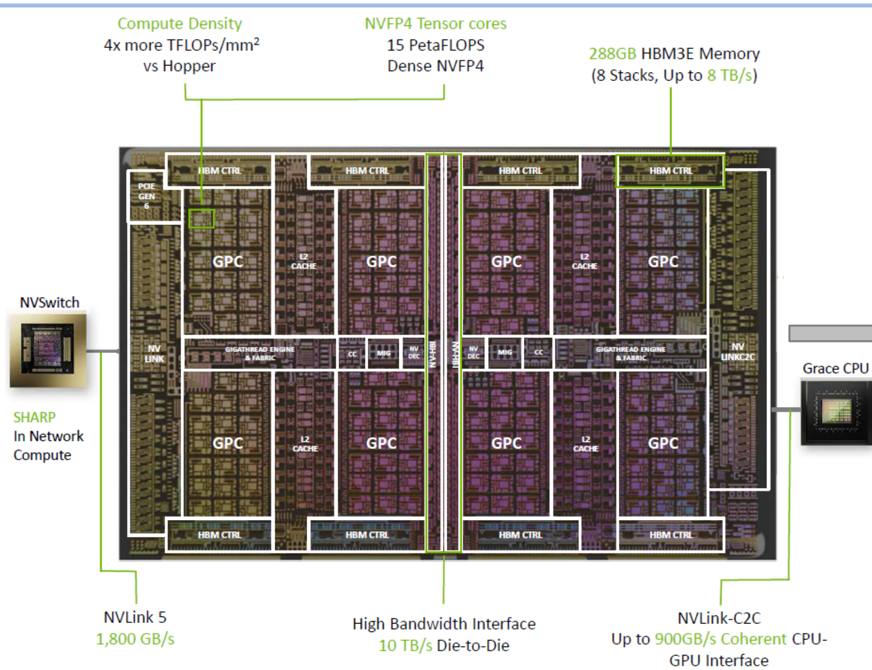
	Chip Architecture	Rack Architecture

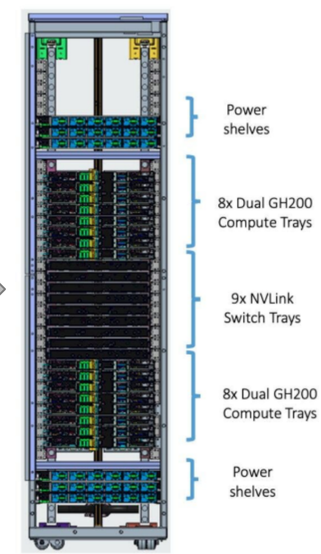
TPU7x Ironwood





Nvidia Blackwell





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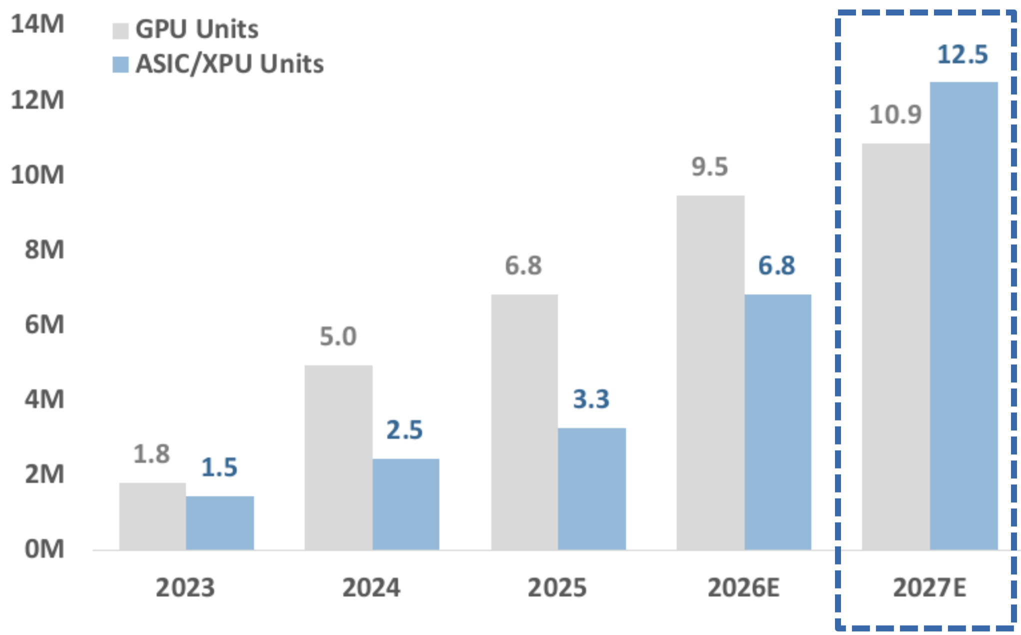
AI ASIC Unit Shipments Forecast to Exceed GPU Units by 2027

AI accelerators units (MM)	2023	2024	2025	2026E	2027E
NVIDIA GPUs	1.7	4.5	6.2	8.9	9.9
AMD GPUs	0.1	0.5	0.7	0.6	1.0
Google TPUs	1.2	1.7	1.8	4.5	8.0
AWS Inferenta + Trainium	0.3	0.8	1.5	1.9	3.3
Meta MTIA	0.0	0.0	0.0	0.3	0.5
Microsoft MAIA	0.0	0.0	0.0	0.2	0.7
Total	**3.3**	**7.4**	**10.1**	**16.3**	**23.3**
Growth Y/Y%		*128%*	*36%*	*62%*	*43%*
GPU % total units	55%	67%	68%	58%	47%
ASIC/XPU % total units	45%	33%	32%	42%	53%



Source: Company reports, J.P. Morgan research

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Custom Chip (ASIC) Market Experiencing a Resurgence in Activity as Large OEMs, Cloud, and Hyperscalers Look to Differentiate at the Silicon Level: $60-70B Opportunity in CY26

- Demand is rising for custom ASICs because many of the large OEMs/CSPs/Hyperscalers are looking for more differentiation, better performance, lower power consumption, and overall lower cost of ownership versus off-the-shelf chip solutions (or ASSPs) – Broadcom (#1 80-85% share high-end ASIC mkt) and Marvell (#2 10-12% share high-end ASIC mkt) should continue to dominate this opportunity.
- These same customers do not have the capabilities to do large, complex system-on-a-chip (SOC) designs, nor do they have the broad IP portfolio of on-chip design blocks, like high-speed SERDES capabilities or high-speed memory interface technology. They need to engage with semiconductor companies that have the IP and chip design expertise.
- The digital custom AI ASIC market is a ~60-$70B market opportunity in CY26 growing at a 40-50%+ CAGR over the next few years :
  - Cloud/Hyperscale ASICS (AI processors, SmartNICs, Security/Video processors, Networking/Storage acceleration)
- **We estimate Broadcom will drive $60B+ in total AI revenue in FY26 (up significantly from ~$20B in FY25) as new products/programs ramp (Meta MTIA 3nm ASIC programs, Google TPUv7/V8 3nm, Anthropic (TPU), OpenAI, and Softbank/ARM)….tracking $150B+ AI revs in FY27**
- **We expect Marvell to drive ~$9.3B of data center revenue in CY26 (up from ~$6.1B in CY25), and ~$14.6B in CY27 – strong optical DSP shipments (800G/1.6T, coherent lite, initial CPO ramp) and continued Amazon Trainium 3 and 4 ASIC engagement and start of Microsoft 3nm Maia ASIC ramp….overall 25+ XPU/XPU attach ASIC wins.**

Snapshot of High-Profile Custom ASIC Programs: AVGO and MRVL

ASIC Customers	Programs	Technology	Status
Cloud Titan A	AI Chip	28nm Technology	Deployed
Cloud Titan A	AI Chip	16nm Technology	Deployed
Cloud Titan A	AI Chip	16nm Technology	Deployed
Cloud Titan A	AI Chip	7nm Technology	Deployed
Cloud Titan A	AI Chip	5nm Technology	Deployed
Cloud Titan A	AI Chip	3nm Technology v6	Ramping Now
Cloud Titan A	AI Chip	3nm/2nm Next Gen v7	Tape Out 1H25, Ramp 2H26
Cloud Titan A	AI Chip	2nm/sub-2nm Next Gen v8	CY27/CY28
Cloud Titan A	VCU Chip	12nm/5nm Technology	Deployed/In Design
Cloud Titan A	Switching	7nm technology	Deployed
Cloud Titan A	ARM CPU	5nm Technology	2024
Cloud Titan B	DPU	7nm/5nm/3nm	2021/2022/2023
Cloud Titan B	Video Trans	7nm technology	2021/2022
Cloud Titan B	Storage	5nm	2023
Cloud Titan B	Security	7nm technology	2021
Cloud Titan B	AI Chip	7nm and 5nm	Deploying
Cloud Titan B	AI Chip	3nm Technology	End CY25 ramp
Cloud Titan B	AI Chip	3nm Technology	Mid CY26 ramp
Cloud Titan B	AI Chip	2nm Technology	CY27 ramp
Cloud Titan C	Security	7nm technology	2020/2021
Cloud Titan C	DPU	7nm/5nm technology	2022/2024
Cloud Titan C	Storage	5nm technology	2023
Cloud Titan C	AI Chip	3nm Technology	CY26 ramp
Cloud Titan C	AI Chip	2nm Technology	CY27 ramp
Cloud Titan D	AI Chip	5nm technology	2024/2025
Cloud Titan D	AI Chip	3nm Technology	CY26 ramp
Cloud Titan D	AI Chip	2nm Technology	CY27 ramp
Cloud Titan D	Storage	5nm technology	2023/2024
AI Compute OEM (OpenAI)	AI Chip	3nm/2nm 3DSOIC	2026
SoftBank/Arm	AI Chip	3nm/2nm 3DSOIC	2026
Asia Hyperscaler#2	AI Chip	3nm	CY26 ramp
Asia Hyperscaler#3	AI Chip	3nm	CY27 ramp

Source: JP Morgan Research

Broadcom ASIC Pipeline:

100+ Cumulative 7nm/5nm/3nm/2nm Designs

Powerful 2nm/3nm ASIC platform (faster time to market):

* 50-120B+ transistors per chip
* 2nm/3nm/5nm chiplet architecture
* 50/100/200G Proven SERDES I/O
* Broadest IP Portfolio
* Adv Pkg (HBM 3/4, 2.5/3D SOIC)
* Co-pkg Electro/Optical (CPO)

Marvell ASIC Pipeline:

70+ Cumulative 12nm/5nm/3nm/2m Designs

Starting to Engage on <2nm

* 50-120B+ transistors per chip
* 50/100G Proven SERDES I/O
* SRAM memory IP (LPU)
* Broad IP Portfolio
* Adv Pkg

AI Custom Chip (ASIC) Beneficiaries: Broadcom and Marvell

Broadcom AI ASIC Pipeline

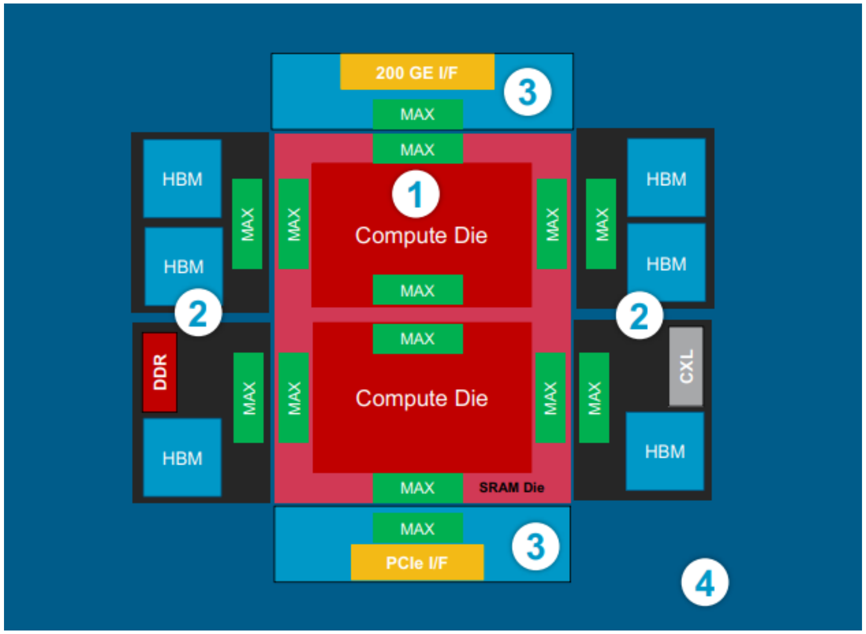
	ASIC Supplier	Generations Won	Ramp Timing/Duration
Google TPU AI ASIC processor family	Broadcom 7nm, 5nm, 3nm, 2nm	V1, V2, V3, V4, V5, V6, V7, V8	Ramping now through CY28
Meta MTIA AI ASIC processor family	Broadcom 7nm, 5nm, 3nm, 2nm	Gen 1, Gen2, Gen 3 and follow-ons	Ramping now through CY28
Bytedance AI Video/AI Networking	Broadcom 5nm, 3nm	Gen 1, Gen2 and follow-ons	Ramping now through CY28
OpenAI XPU AI ASIC processor family	Broadcom 2nm and 3nm	Gen1 and Gen 2 on 3DSOIC pkging	Ramping CY26-CY29
SoftBank/Arm XPU AI ASIC processor family	Broadcom 2nm and 3nm	Gen 1 and Gen 2 on 3DSOIC pkging	Ramping CY26-CY29
Anthropic/TPU Rackscale	Broadcom 3nm	TPUv6p - Ironwood	Ramp 2H CY26
Customer #7 AI ASIC XPU (Asia Hyperscale Customer	Broadcom 3nm, 2nm	Gen 1, Gen 2	Ramping End 26
Customer #8 AI ASIC XPU (Asia Hyperscale Customer	Broadcom 3nm, 2nm	Gen 1, Gen2	Ramping CY27

Marvell AI ASIC Pipeline

Amazon AI ASIC processor family	Marvell 5nm/3nm/2nm	Gen 2, Gen 3, Gen 4 and follow-ons	Ramping Now
Microsoft Maia AI ASIC processor family	Marvell 3nm/2nm	Gen 2 and follow-ons	Ramping End CY26
Google AI ARM CPU processor family	Marvell 5nm/3nm	Gen 1 and follow-ons	Ramping Now
Cloud/Hyperscale FBNIC (SmartNic)	Marvell 5nm/3nm	Gen 1 and follow-ons	Ramp 2H25
Other XPU Attach (SmartNIC, Fabric, Memory)	Marvell 3nm/2nm	Gen 1 and follow-ons	Ramping CY26

Source: JP Morgan Research

Broadcom's Powerful 3D SOIC ASIC Reference Platform / Marvell Custom HBM Designs

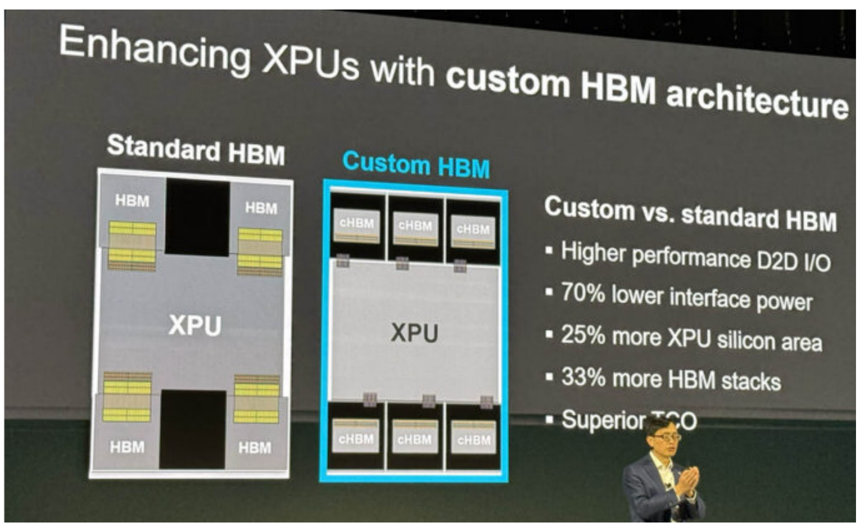


Source: Broadcom and J.P. Morgan Research

Broadcom Has Developed a 2nm/3nm AI ASIC Reference Platform to Enable Customers Fast Time to Market:

- 2nm/3nm/5nm compute die
- 100/200Gbps I/O die
- 2.5D/3D SOIC (chip stacking)
    - 2nm/3nm chip stacking
    - **Advanced substrate manuf capability in CY26**
- Chip-to-Chip I/O connectivity
- AI/Compute/IO/Memory/Interface IP
- **Rackscale system expertise ramping CY26**

Broadcom is working with 3 of its 5 AI ASIC customers on next-gen 3D SOIC chip stacking ASIC programs



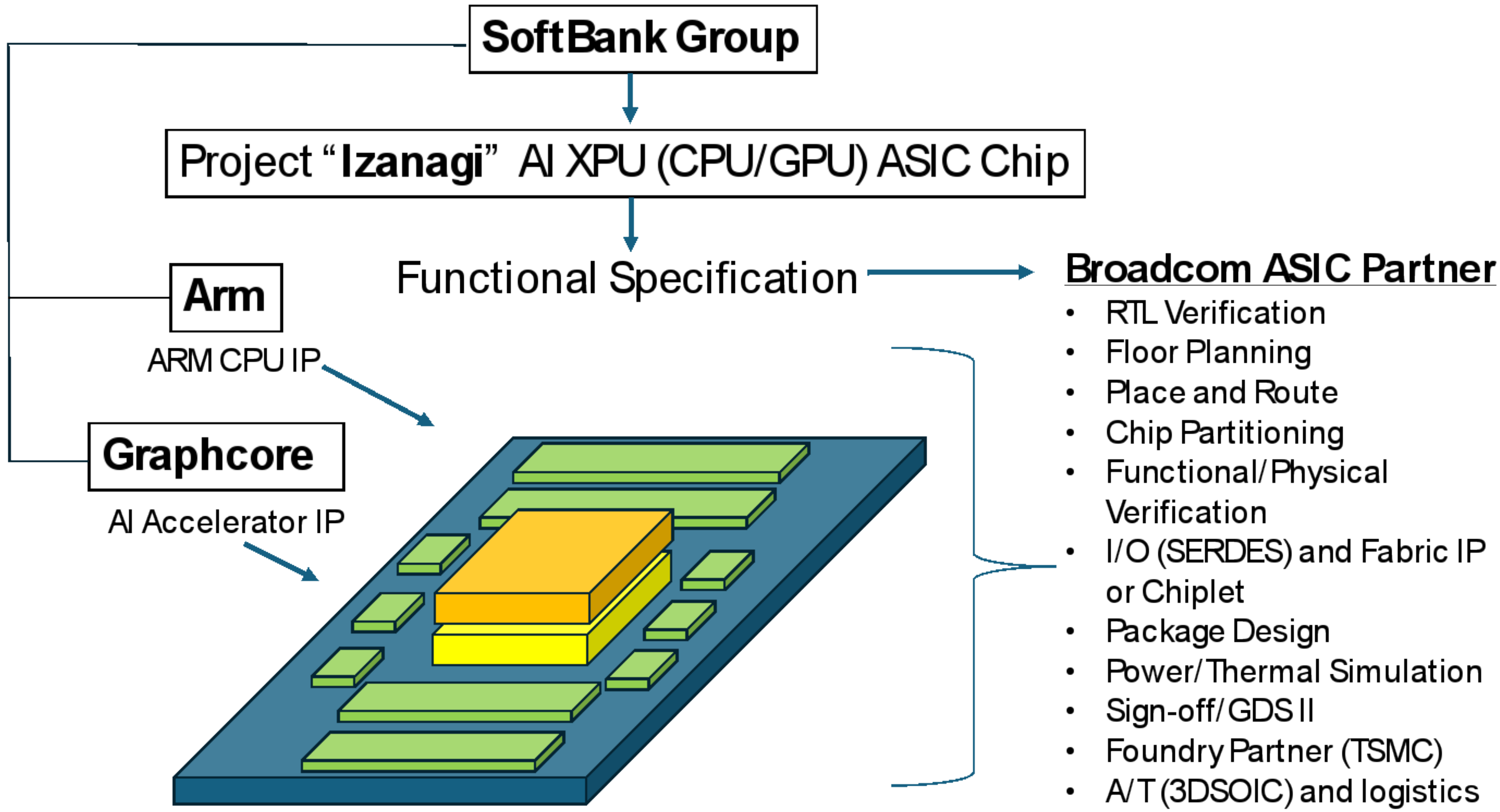
Source: Marvell and J.P. Morgan Research

Marvell has a strong IP portfolio of 5nm, 3nm, and 2nm

Recently unveiled HBM memory IP differentiation that drives:

- 33% more HBM stacks per package
- 70% lower interface power
- 25% more XPU silicon area
- **Marvell has won numerous HBM4 ASIC logic base die programs with DRAM suppliers**

Broadcom AI ASIC Customer SoftBank/Arm AI XPU

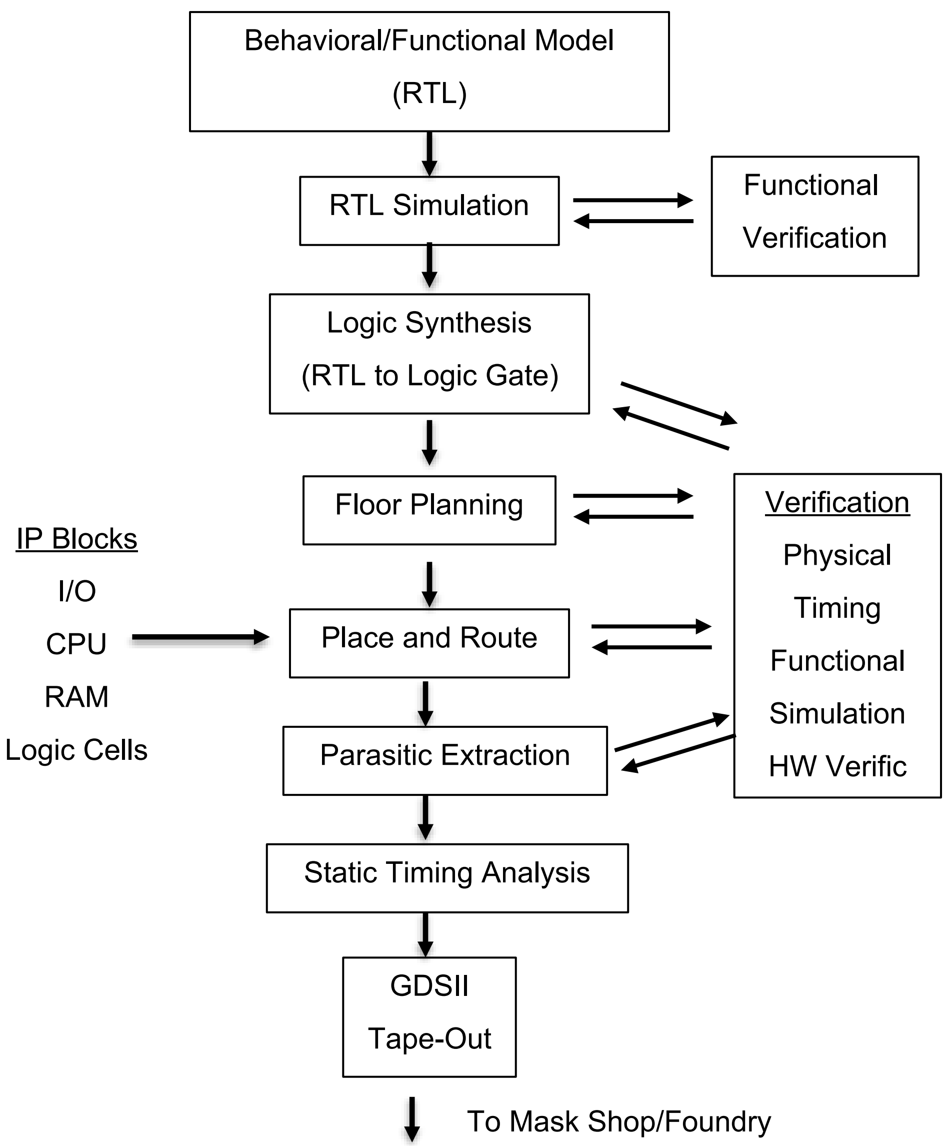


Source: J.P. Morgan Research

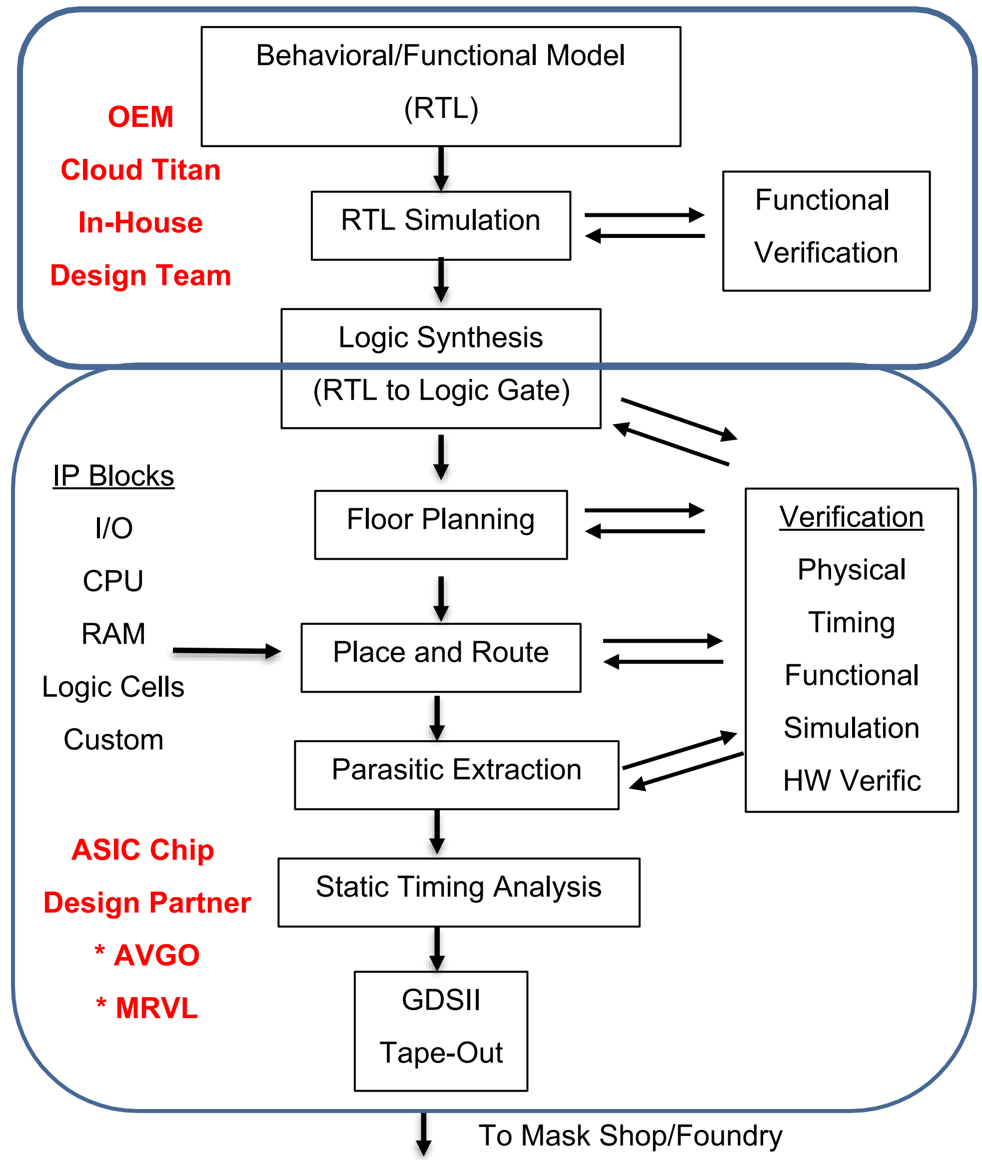
Meta/ARM CPU Announcement Is NOT the Broadcom ASIC – Meta Project Is CPU-only….The Broadcom ASIC Is a Full-Blown AI XPU (CPU+AI Accelerator)

Merchant Chip Design vs. ASIC Chip Design vs. COT Chip Design

Merchant (Semi Co.) Chip Design Flow

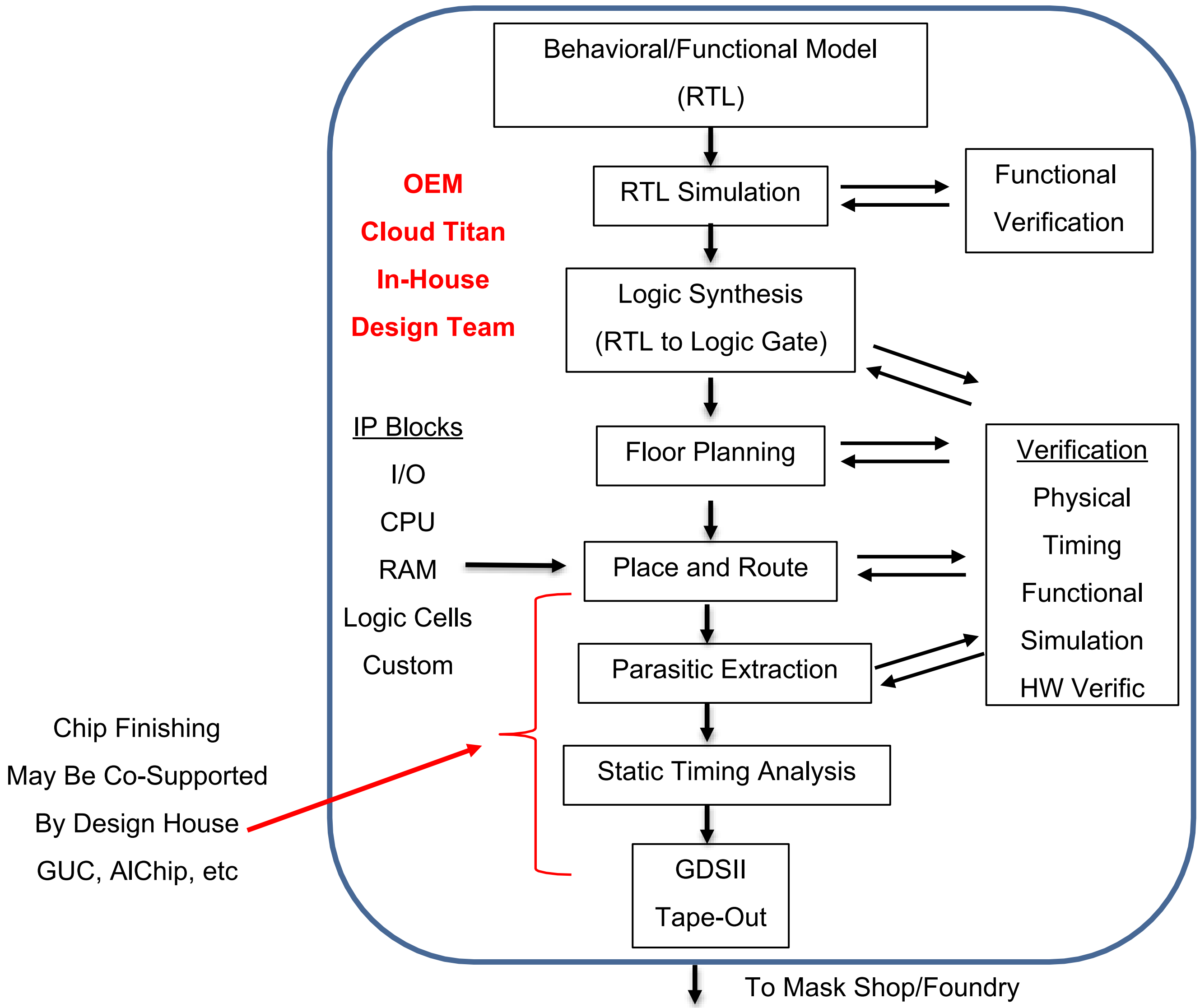


ASIC Chip Design Flow



Merchant Chip Design vs. ASIC Chip Design vs. COT Chip Design

COT Chip Design Flow (System OEM/Cloud Titan Does 85-100% of Design And IP)



Example ASIC Designs:

1) Google TPU (AVGO ASIC)
2) Google VCU (MRVL ASIC)
3) Meta TPU (AVGO ASIC)
4) AMZN 3rd Gen (MRVL ASIC)
5) Google CPU (MRVL ASIC)
6) Cisco Switching (AVGO/MRVL)
7) Nokia 5G BTS (AVGO/MRVL)
8) Samsung 5G BTS (MRVL ASIC)

Example COT Designs:

1) Apple A and M series CPU
2) AMZN 1st/2nd Generation SoC
3) Tesla DOJO AI SoC
4) Cisco - Cloud Scale SoC

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Near-Term Update on AVGO/MRVL ASIC Pipelines

Broadcom Update On ASIC Pipeline

- Google TPU orders continue to add to the CY27 backlog - currently around 6.5M+ V7/V8 shipments….~$100B in revenues
- Google Near-term – 3K wafer starts per week TPUv7 (Ironwood) – sets up for strong 2H26 (along with initial V8 ramp)…support Google Internal and Anthropic.
- Meta ramping first 3nm program (Athena) NOW, “Iris” 3nm Mid-CY26, “Arke” End CY26, “Astrid” 1H27 - added new 2nm program for 2H27 ramp…..total five programs – 1GW CY27
- OpenAI (2nm/3nm) and Softbank/ARM XPU first silicon both out of fab – functionality looks good….on track for end of year/CY27 ramp – OpenAI 1GW in CY27
- Google/AVGO assessing v8i “next-gen” – 4 compute die, 12 HBM stacks- extend life of TPUv8i for 6 more months….then ramp next gen v9/v10 2nm TPU (4 compute, 16 HBM)…either strategy will NOT result in revenue “air-pocket” in CY28 (70%+ growth CY28)

Marvell Update on ASIC Pipeline

- XPU ASIC Trainium 3 (3nm) production commenced last quarter – on track to ramp mid-CY26…..Trainium 4 (2nm) on track to ramp 2H CY27
- Celestial CPO solution (Tied to Trainium 4) have seen upside to 2H27 orders
- XPU ASIC Microsoft Maia 3nm – taping out soon – program set to ramp beginning CY27 (full ASIC engagement - FE/BE design)
- XPU attach: multi-billion dollar /multi-year win for Google SmartNIC/DPU ASIC – ramp CY27 - CXL controller ASIC – ramp 2H26
- XPU attach: **early engagement** on “LPU” offload inference engine (recall MRVL did 1st gen Groq LPU ASIC due to strong SRAM memory IP) – No wins yet, but expected

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