

June 2, 2026 04:22 PM GMT

Greater China Technology Semiconductors | Asia Pacific

Key Computex Takeaways: Agentic AI, TSMC capacity and MediaTek's AI PC chips

Agentic AI and CPU servers dominated the Computex keynote discussions. Nvidia indicated that TSMC's capacity can support robust growth for Nvidia in 2027.

Agentic AI compute key focus: In their keynotes, Nvidia, Arm and Qualcomm emphasized Arm-based server CPUs to support future agentic AI demand, echoing our report, *Global Tech: Agentic AI – The Surge Begins (11 May 2026)*.

Comments on Nvidia Vera CPU: Ahead of Computex, we published *NVIDIA's Vera CPU and Rubin GPU seen as the main show (27 May 2026)*. At today's investor luncheon, our Nvidia analyst Joe Moore asked CEO Jensen Huang the first question about the US\$20bn Vera CPU revenue assumption. Management indicated that demand spans both AI server head nodes and stand-alone CPU servers. Given its materially better performance than the x86 (see [Exhibit 5](#)), Nvidia can command higher values for Vera, excl. memory sales. Our supply chain checks suggest 2.5mn–4mn units are in preparation. Rubin has already entered fab production with no apparent delays. On CPO (optics) vs. copper, Nvidia indicated that it will adopt CPO only when necessary and rely on copper as long as possible.

Sufficient TSMC capacity: At the 2024 and 2025 Computex events, we asked Jensen Huang about TSMC's pricing and value. This year, we asked whether Nvidia can secure sufficient TSMC capacity for 2027 and whether allocation could affect market share. We also asked – even more importantly – how Nvidia could secure incremental allocation versus competitors.

Nvidia indicated it has sufficient TSMC capacity to support robust growth in 2027. The company has convinced TSMC and other suppliers that demand remains strong. Even as supply expands, demand will likely still exceed supply in 2027. Management also emphasized that the AI semiconductor market is growing and does not represent a zero-sum or pure market share competition.

Agentic AI at the edge – do we need a local LLM/agent: Nvidia announced its RTX Sparks AI PC WoA SoC in its keynote, jointly designed with MediaTek. We flagged this 9 months ago in our [MediaTek report](#), saying "Nvidia/MediaTek WoA AI PC keeps being pushed out – now to 2H26. For N1X, we think the new timing of product launch would be next year's Computex in June (vs. the CES in January), given that Microsoft's new AI Windows system will be more of a 2H26 rollout. Moreover, the new x86 SoC will fuse an Intel CPU + Nvidia RTX GPU chiplet via NVLink". We do not see this launch as a surprise. Investors are asking about the volume of RTX Sparks in 2026 and whether edge AI compute is necessary for Agentic AI.

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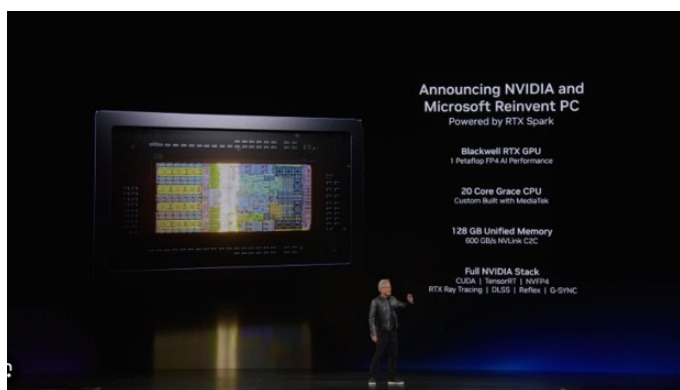


Key takeaways from Computex Day 1 + implications for Greater China semis

Potential volume of Nvidia RTX Spark:

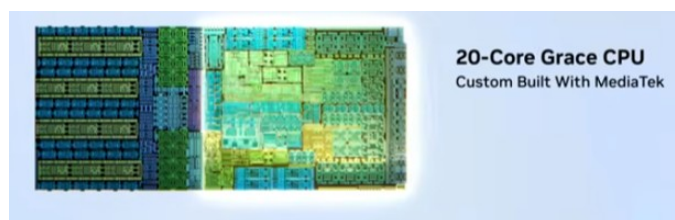
Our checks with PC brands at this year's Computex suggest AI PCs with N1X will need to price at US\$2,899, while N1 models will be priced at US\$1,799. We therefore estimate ~5mn–8mn units of N1X/N1 SoC shipments in 2026, contributing 5–10% of MediaTek's 2026 EPS, assuming an average US\$40 royalty fee per chip.

Exhibit 1: New AI PC announced by Nvidia (N1X)



Source: Nvidia

Exhibit 2: MediaTek provides 20-core customized Grace CPU for N1X



Source: Nvidia

Exhibit 3: RTX Spark (N1X) provided by MSI (available in 3Q26)



Source: MSI

Exhibit 4: RTX Spark (N1X) provided by ASUS (available in 3Q26)

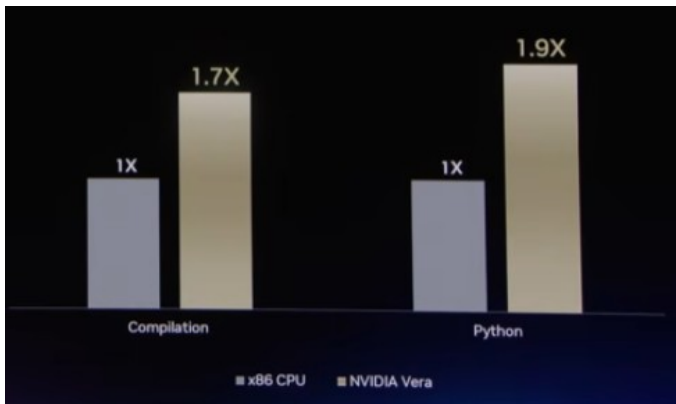


Source: ASUS

Greater China semis in the supply chain:

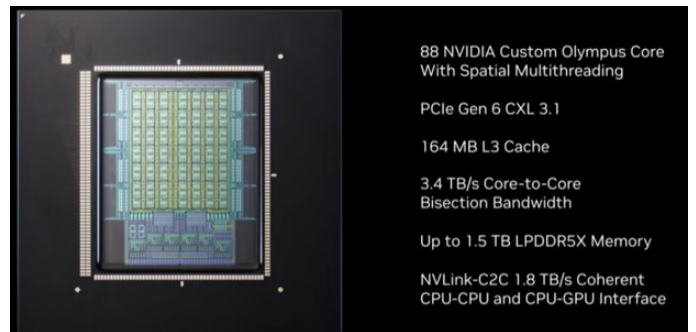
- **Nvidia AI GPU supply chain:** TSMC (foundry), ASE (packaging), KYEC (testing), AllRing (equipment)
- **CPO supply chain:** FOCI (FAU), Himax (WLO), ASE (optical insertion testing), Hon Precision (optical insertion tool)
- **CPU supply chain:** KYEC (Vera and Google CPU test), Aspeed (general server BMC)
- **WoA AI PC:** MediaTek (N1X and N1 chips), Macronix (NOR Flash for AI PC)

Exhibit 5: Vera performance could be 1.8x that of highest-performance x86 CPU



Source: Nvidia

Exhibit 6: Vera CPU cores are not split across chiplets, enabling faster core-to-core connection



Source: Nvidia