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Greater China Semiconductors

The New Tauism: Huawei's Tau Scaling Advances Chip Performance

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CITI'S TAKE

Huawei introduced the Tau (τ) Scaling Law at the IEEE ISCAS on May 25th, a new design philosophy of chip scaling with time (latency reduction) rather than geometry (transistor shrinkage). Exemplified as LogicFolding, Huawei vertically stacked active tiers of logic, analog, and memory circuits using ultra-fine hybrid bonding (at 1.5μ pitch) and claims to achieve 55% increase in transistor density to 238 MTr/mm^2 for the Kirin 2026 chip. While the same geometry constraints remain, we view this a credible design response to China's restriction on advanced nodes and a shift towards innovations in chip/circuit/system designs. We expect providers of advanced packaging equipment and services to be key beneficiaries.

Tau Scaling: scaling of time instead of geometry — On May 25th, Huawei presented at the IEEE ISCAS its Tau (τ) Scaling Law, a new design philosophy of using latency reduction as the primary metric for chip performance. Given Huawei's lack of access to advanced equipment, Huawei aims to narrow the chip performance gap through 3D integration, hybrid bonding, logic/memory fusion, optical I/O, backside power, and EDA flows. Huawei targets to achieve 1.4nm-equivalent logic density by 2031.

LogicFolding: vertical stacking of mobile SoC — The Tau Scaling was implemented first on Huawei's mobile SoC using LogicFolding methodology. Logic, analog, and memory circuits across vertically stacked active tiers are bonded using ultra-fine-pitch hybrid bonding, acting as a single continuous fabric. The Kirin 2026 chip achieved a 1.5μ hybrid bonding pitch. Huawei claims a 55% increase in transistor density (from 155 to 238 MTr/mm^2) and a 41% power-efficiency gain at a fixed device node, and forecasts transistor density to >400 MTr/mm^2 from 2026 to 2035.

Tau Scaling achievement and limitation — We view Huawei's Tau Scaling a credible design response to China's restriction on advanced nodes. Huawei pushes ahead chip performance through innovations across transistor, circuitry, chip, and system levels. That said, the geometry shrinkage remains given lack of EUV lithography. The 238 MTr/mm^2 density in 3D does not equate to density in planar designs. 3D design could also lead to new challenges in thermal constraints and EDA limitations.

Implications — We believe Tau Scaling signals a shift towards chip/circuit/system design innovations, which could become more popularized if proven effective. We expect key beneficiaries in 1) **advanced packaging equipment** – especially providers of hybrid bonders, 2) **OSAT** – given rising packaging complexity, 3) **foundry** – given advanced chip design, and 4) **EDA** – to support 3D design. Within our coverage, we favor **ASMPT** given its broadening advanced packaging solution offerings.

See Appendix A-1 for Analyst Certification, Important Disclosures and Research Analyst Affiliations.

Figure 1. Comparison – Geometry Scaling vs. Tau (Time) Scaling

Geometry Scaling	Tau (τ) Scaling
Transistor shrinkage	Signal latency reduction
Transistor density	Compute + memory + interconnect efficiency
2D planar scaling	3D stacking + hybrid bonding
Advanced foundry capability	Advanced packaging, EDA design, system architecture
Device performance optimization	Full stack co-optimization

Source: Citi Research

Figure 2. Huawei Kirin Performance Comparison

Year	SoC	Architecture	Frequency (GHz)	State
2023	Kirin9000s	Planar	2.6	Mass production
2024	Kirin9020	Planar	2.65	Mass production
2025	Kirin9030 pro	Planar	2.75	Mass production
2026	Kirin 2026	LogicFolding	3.1	Silicon
2027	Kirin 2027	LogicFolding	3.39	Silicon
2028	Kirin 2028	LogicFolding	3.71	Pre-silicon
2029	Kirin 2029	LogicFolding	4	Pre-silicon

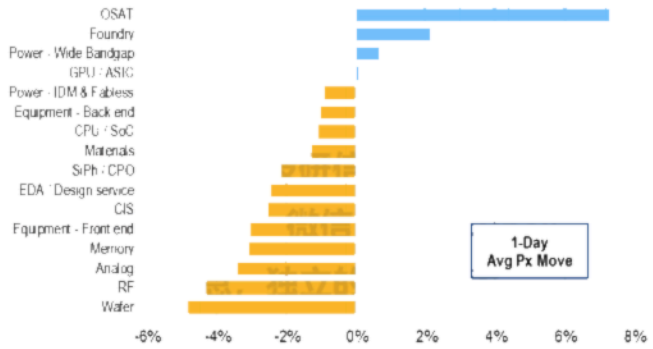
Source: Citi Research

Figure 3. Share Price Movement – by Sectors

26-May-2026	1D	1W	1M	3M	6M	12M
Foundry	2.2%	21.4%	37.3%	29.1%	56.3%	178.4%
OSAT	7.3%	28.2%	65.5%	41.5%	85.9%	132.9%
Equipment - Front end	-3.0%	5.8%	41.9%	32.7%	74.0%	149.8%
Equipment - Back end	-1.0%	10.1%	47.8%	67.3%	193.3%	355.0%
CPU / SoC	-1.1%	4.9%	26.3%	27.7%	55.9%	87.7%
GPU / ASIC	0.1%	3.4%	12.8%	46.0%	9.9%	37.2%
Memory	-3.1%	4.2%	63.3%	65.4%	97.5%	297.4%
SiPh / CPO	-2.1%	5.2%	27.0%	88.9%	195.7%	722.3%
Analog	-3.4%	2.9%	26.7%	46.5%	70.7%	83.1%
Power - IDM & Fabless	-0.9%	10.4%	30.7%	11.8%	58.6%	95.8%
Power - Wide Bandgap	0.7%	1.3%	26.2%	24.8%	36.3%	45.8%
CIS	-2.5%	2.3%	13.3%	-2.6%	2.8%	1.3%
RF	-4.3%	-4.0%	10.7%	15.9%	26.6%	32.2%
EDA / Design service	-2.4%	11.6%	30.7%	14.1%	37.2%	115.4%
Wafer	-4.8%	-7.7%	24.9%	14.6%	33.9%	48.3%
Materials	-1.3%	0.0%	19.1%	38.6%	104.1%	155.7%

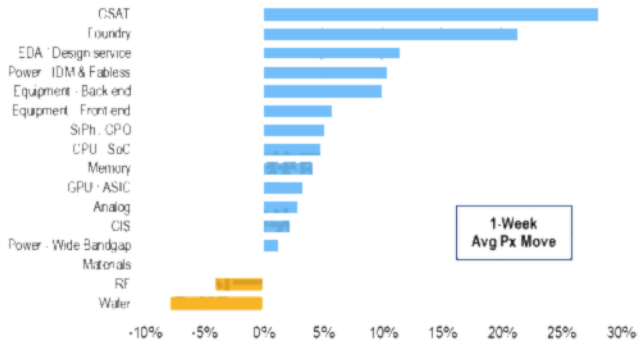
Source: dataCentral, Citi Research

Figure 4. Share Price Movement – 1 Day



Source: dataCentral, Citi Research

Figure 5. Share Price Movement – 1 Week



Source: dataCentral, Citi Research

ASMPT

(0522.HK; HK$204.6; 1; 26 May 26; 16:10)

Valuation

Our target price of HK$180 is based on peak valuation of 37x 2027E P/E. We view the peak valuation as justified because we expect strong revenue and earnings recovery driven by: 1) AI-driven advanced packaging order wins, including TCB for HBM and CoW applications; and 2) ongoing recovery of mainstream SEMI and SMT. Potential sales of SMT business could solidify its market position as a leading provider of advanced packaging solutions, leading to valuation re-rating beyond its historical range.

Risks

Downside risks to our target price being achieved include: 1) a slowdown in AI infrastructure outlook with delayed investment; 2) TCB market share loss at key customers; 3) reduced TCB demand due to alternative technologies, such as hybrid bonding; 4) intensifying industry competition; and 5) export restriction extending to back-end equipment.